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EXTENDABLE PHASED-ARRAY PLATFORM INTEGRATED CIRCUITS (EPIC)

Brian A. Floyd

North Carolina State University

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// Signature//
PAUL M. WATSON, Program Manager
Integrated Circuits & Microsystems Branch
Aerospace Components & Subsystems Division

// Signature//
ATTILA A. SZEP, Chief
Integrated Circuits & Microsystems Branch
Aerospace Components & Subsystems Division

// Signature//
RANDALL D. DEPPENSMITH, Lt Col, USAF
Deputy
Aerospace Components & Subsystems Division
Sensors Directorate

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2701 Sullivan Dr., Ste 240, Campus Box 7514
Raleigh, NC 27695-7003

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14. ABSTRACT
A platform approach to phased-array architecture was investigated. The platform consists of reusable 15-32GHz transceiver cores in 45nm SOI CMOS and 15-100GHz beamforming extenders in SiGe. The receiver core was realized as a four-phase passive mixer-first receiver, operating across 6-33GHz, achieving a measured 5-9dB noise figure, 20dB conversion gain, -12 to -3dBm input-referred compression point, and consuming 110-220mW. This meets program goals and is the highest and broadest operating frequency for a passive mixer-first receiver. The transmitter core was realized as an active Gilbert-cell mixer and balanced power amplifier. In simulation, the transmitter core achieves 17-19dBm output compression and operates across 20-33GHz. This hardware is still in fabrication. Three extenders were realized, including a measured 28GHz four-element transceiver array, a measured 60GHz four-element receiver array, and a simulated 80GHz single-element transmitter, still in fabrication. Full platform demonstrations including the core plus the extenders are in progress.

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1. PROGRAM OVERVIEW

1.1 Summary

North Carolina State University (NCSU) investigated a platform approach to reusable phased-array intellectual property (IP) design, wherein the system is partitioned into a flexible and reusable "core" transceiver plus interchangeable millimeter-wave (mm-wave) beamforming "extenders", as illustrated in Figure 1. This is motivated from the following reasons. The design of an mm-wave phased-array communication system for defense application is a difficult, time-consuming, and expensive task. Each new system often requires the design or redesign of a significant portion of a radio to meet performance and functionality requirements. Also, realizing highly integrated system-on-chips requires advanced complementary metal-oxide-semiconductor (CMOS) technology but leads to long, expensive development cycles. If reusable IP can be found for the transceiver core, then that core can be leveraged across many systems and applications and save both development time and money.

Our approach, entitled **Extendable phased-array Platform ICs (EPIC)**, centers on a flexible fifth-generation cellular (5G) IP core designed to be reused in any phased-array platform solution operating at 15 to 200 GHz. This project includes the architecting of a 15-32 GHz CMOS multi-purpose transceiver core and system demonstration using both existing and newly created prototype beamformers at 28, 60, and 80 GHz. The project also includes comparisons between this platform approach to dedicated custom designs to evaluate performance, area, power, and design-time trade-offs. The project is organized into three thrusts, as follows: (1) multi-purpose transceiver CORE development; (2) mm-wave beamformer EXTENDER development, leveraging industry activities; and (3) mm-wave phased-array PLATFORM evaluation.

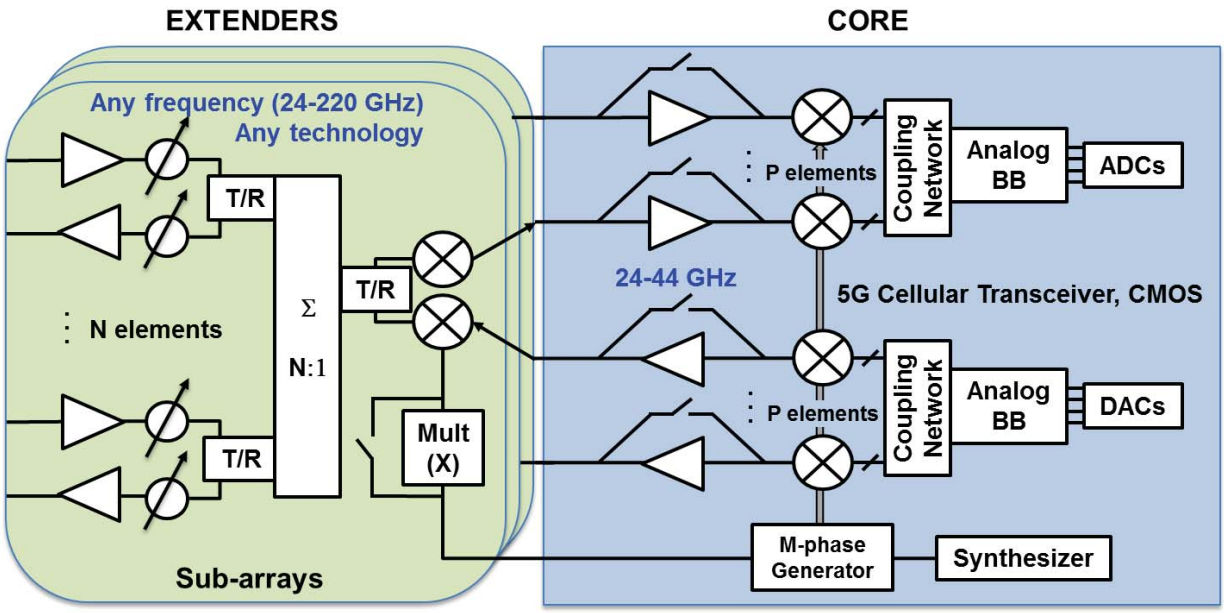


Figure 1: Block Diagram of the Extendable Phased-Array Platform IC System Concept
Including beamformer extenders operating at any frequency and technology and a reusable IP core based around a 5G transceiver.

1.2 System Architecture

The reusable CORE is a wideband 15-32 GHz transceiver covering 5G cellular bands and providing up- and down-conversion and all analog-signal processing for aggregated sub-array signals. A standardized interface for interfacing between the CORE and beamformers allows for "plug and play" exchangeability between CORE and EXTENDER. The system operates with a single frequency synthesizer, simplifying the frequency plan, where a global local oscillator (LO) signal is used within both the CORE and the EXTENDER.

Each receiver CORE includes widely tunable direct downconversion to analog baseband. In our system, this is realized using passive mixers. An optional bypassable low-noise amplifier (LNA) can be used to reduce noise figure (NF) at the expense of reduced linearity. As we will show, this appears to provide limited value, as the mixer-first receiver CORE can provide higher dynamic range with acceptable NF. Each transmitter CORE includes widely tunable direct upconversion to 15-32 GHz. In our system, this is realized using an active, Gilbert-cell mixer to provide gain and isolation between baseband and the output. An optional bypassable power amplifier (PA) can be used to increase output power. Although data converters and a frequency synthesizer are shown in the CORE in Figure 1, we did not include those in our work to contain program scope. We focused instead on the key radio frequency (RF) functional elements.

EXTENDERs are attached to extend the capabilities of the CORE to include additional beamforming, higher performance amplifiers, and/or higher frequency of operation. These EXTENDERS form N-element sub-arrays for the system, whereas "P" COREs can be used (one per sub-array); hence, an overall N×P element scaled solution can be achieved.

As proposed, EPIC was to enable three different architectures or "modes", as shown in Figure 2.

Mode 1: A direct-conversion architecture can be realized for 15- to 32-GHz operation, where the EXTENDER adds beamforming capabilities and enhanced RF performance but operates at the same frequency as the CORE.

Mode 2: A sliding- intermediate frequency (IF) architecture can be realized for >32-GHz operation, where the EXTENDER adds beamforming and frequency conversion.

Mode 3: A subharmonic architecture can be realized for >32-GHz operation, where the EXTENDER adds beamforming and relies on 3rd-harmonic excitation of mixers within the CORE. Our research on the CORE has shown that this is not advisable.

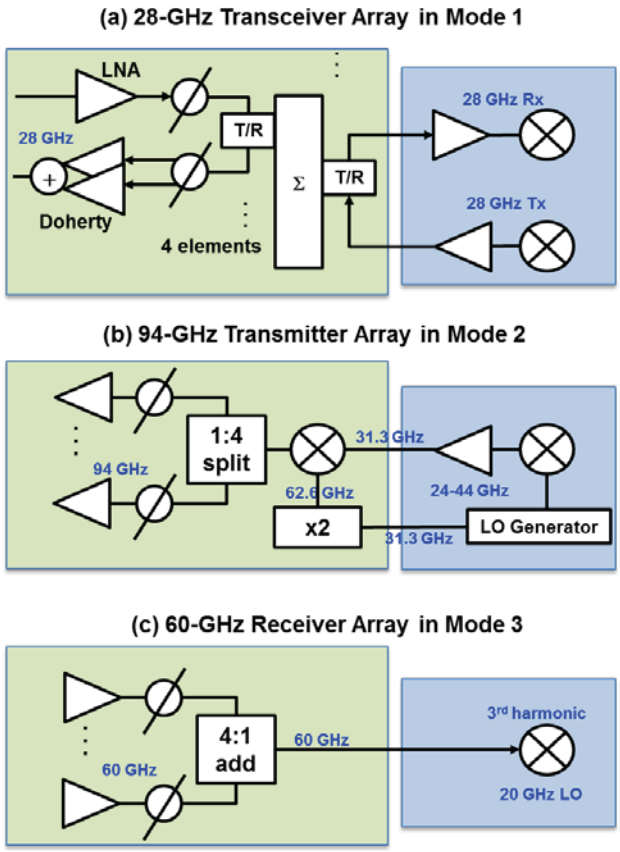


Figure 2: Example Operational Modes, with EXTENDERS in green and CORE in blue
(a) Diagram of mode 1 for 28-GHz transceiver array, (b) diagram of mode 2 for 94-GHz transmitter array, and (c) diagram of mode 3 with for 60-GHz receiver array.

1.3 Program Term and Organization

This Defense Advanced Research Projects Agency (DARPA) seedling project ran from May 9, 2016 through July 9, 2018 for a total of 26 months. This includes an eight-month no-cost extension over the original 18-month contract. This no-cost extension was needed to accommodate delays encountered with tape-outs and design kits.

Our work was organized into three thrusts:

Thrust 1: Transceiver CORE – The goal of this thrust is to design and realize a multi-purpose IP CORE which has the flexibility to work with any beamformer at any frequency.

Thrust 2: EXTENDER Development – The goal of this thrust is to design and evaluate beamforming extenders operating at 28, 60, and >80 GHz. The 28 and 60 GHz EXTENDERS are realized under industry-funded parallel project. The >80 GHz EXTENDER is realized within EPIC. One unique aspect of this program organization, which was requested by DARPA, was an exploration of how to leverage commercial activities for both IP-reuse as well as research leverage. Here, we leveraged a 28 GHz beamformer [Yeh17] which was developed under

funding from Analog Devices Inc. and a 60 GHz beamformer [Gre18] which was developed under funding from Samsung and the Semiconductor Research Corporation (SRC).

Thrust 3: PLATFORM Integration and Demonstration – The goal of this thrust is to evaluate phased-array PLATFORMS comprising the multi-purpose IP CORE and mm-wave EXTENDERS. Performance will be evaluated according to program metrics.

1.4 Program Challenges

First, we encountered technical challenges in (a) the design of our CORE transceiver which resulted in additional hardware iterations and (b) the design of our highest frequency EXTENDER which resulted in shifting from 150 GHz to 80 GHz to allow re-use of existing hardware blocks [Fuj17]. As will be shown, the operation of the broadband passive-mixer receiver CORE is highly dependent on high-quality LO signals. We required multiple iterations to get this LO network functioning properly to support 5-32 GHz. For our 150 GHz EXTENDER, we saw large modeling errors which, while fixable, was avoided by shifting from 150 GHz to 80 GHz and from SiGe 9HP to SiGe 8HP. The schedule was still delayed as a result.

Second, we encountered significant process design kit (PDK) challenges for 45nm RF silicon-on-insulator (RFSOI) from GlobalFoundries (GF). This included a shift from IBM's CMOS-12S PDK to GFs first 45RFSOI PDK, a shift to a revised GF 45RFSOI PDK in which mm-wave enablement was introduced which replaced some of our custom components, and a shift to a new required metal stack in GF 45RFSOI. Altogether, this led to postponed tape-outs and significant repeated work, costing about six months of development time. Consequentially, the final version of our transmitter CORE is still in fabrication.

Finally, we encountered staffing challenges, where the Thrust 3 platform leader, research professor Morteza Abbasi left NCSU in December 2017. His expertise included mm-wave packaging and assembly and full system evaluation. As a result of this, as well as the status of our transceiver CORE, we have not yet demonstrated assembled phased-array platforms. This work will continue beyond the period of this contract and we plan to release a supplement to this final report once that work is completed.

1.5 Program Key Accomplishments

Key accomplishments are as follows:

- In Thrust 1, we investigated and demonstrated multiple generations of mixer-first receivers for operation in the 5-35 GHz range. Most significantly, our final receiver core achieves all original EPIC program goals. This four-phase mixer-first receiver operates across 6 to >33 GHz with high frequency selectivity provided around the frequency band set by the LO frequency and the baseband amplifier bandwidth. *This four-phase receiver exhibits the highest and broadest operating frequency range to date for mixer-first receivers.* We believe that this receiver is a very useful component for both the EPIC platform as well as broadly tunable, frequency-selective digital beamformers.

- In Thrust 1, we investigated and demonstrated an eight-phase mixer-first receiver which operates across 10-16 GHz, which is the *highest frequency range to date for eight-phase systems to our knowledge.* Despite this, our data indicate that this eight-phase system does not outperform the four-phase system, due to reduced RF performance coming from imperfect LO signals.
- In Thrust 1, we determined that the mixer-first four-phase receiver will outperform an LNA-first system. This is based on measured data for our Gen-2 receiver as well as measured data for a 24-44 GHz broadband LNA [Cha18] implemented in this program.
- In Thrust 1, we have shown *through simulation* a broadband transmitter which can achieve output power of 17-19 dBm across 20-33 GHz. If replicated in measurement, this should represent the highest output power for a 5G transmitter system to date.
- In Thrust 2, we demonstrated a 28-GHz transceiver beamformer which achieves compact area per array tile and state-of-the-art RF performance [Yeh17].
- In Thrust 2, we demonstrated a 60-GHz receiver beamformer which achieves accurate phase shifting across 57-67 GHz, state-of-the-art RF performance, and novel built-in-self test capabilities [Gre18].

1.6 Patents, Publications, and Deliverables

We have not filed any patents based on this work. A list of the related publications is as follows:

[Cha18] V. Chauhan and B. Floyd, "A 24-44GHz UWB LNA for 5G cellular frequency bands," *IEEE Global Symp. Millimeter-Waves*, May 2018.

[Gree18] K. Greene, V. Chauhan, and B. Floyd, "Built-in-test of phased arrays using code-modulated interferometry," *IEEE Trans. Microw. Theory Tech.*, vol. 66, no. 5, pp. 2463-2479, May 2018.

[Yeh17] Y.-S. Yeh, E. Balboni, and B. Floyd, "A 28-GHz phased-array transceiver with series-fed dual-vector distributed beamforming," *IEEE RF Integrated Circuits Symp.*, June 2017.

We still plan multiple publications related to the CORE and the full platform, including one or more receiver core publications (Gen-2 four phase and Gen-1B eight phase), one or more transmitter core publications (PA and full transmitter), and one or more phased array systems (28 GHz and 80 GHz).

In terms of deliverables, we have provided quarterly technical and financial reports. Hardware deliverables for the full platforms have not yet been provided, as this work is still in progress.

2. THRUST 1A: CORE RECEIVER RESEARCH AND DEMONSTRATION

The goal of this sub-thrust is to design and realize a multi-purpose receiver IP CORE which has the flexibility to work with any beamformer at any frequency. This core can serve as a direct downconversion stage for beamformers which operate at the same frequency as the core (i.e., from 15-32 GHz). Alternatively, the core can serve as a second downconversion stage in a superheterodyne architecture, in which the beamformer includes a first downconversion to an intermediate frequency between 15-32 GHz.

Discussion is organized according to the three generations of receivers which were implemented. A first design and tape-out (Gen-0) was completed in March 2016, prior to start of the DARPA project, and it was measured during the first year of the EPIC program and formed the starting point for our design efforts. A second design and tape-out (Gen-1) was completed in April 2017 with key measurements completed by January 2018. A third design and tape-out (Gen-2) was completed in February 2018 with key measurements completed by August 2018. This illustrates a cycle time for each receiver generation of one year for the 45-nm SOI CMOS technology used for this work.

A summary of the final measured results is given in Table 1. These results will be discussed in detail in the following sections. We see that our final Gen-2 receiver meets all original EPIC program goals, operating over 6-32 GHz as compared to an EPIC goal of 15-32 GHz. Both our Gen-2 four-phase and Gen-1B eight-phase mixer-first receivers *achieve the widest range and highest operating frequency to date*. Also, our research has shown that four-phase operation is superior to eight-phase. Six-phase was not pursued to avoid the need to design high-speed divide-by-three circuits.

Table 1. Comparison of Receiver Measurements to Modified EPIC Targets
(Missed specification in red)

	Gen-0	Gen-1A	Gen-1B	**Gen-2**	**EPIC Target**
Freq. Range	4-17 GHz (Var-A) 15-22 GHz (Var-B)	21-32 GHz	10.5-16 GHz	**6 to >33* GHz (*expect 37GHz)**	**15-32 GHz**
Phases	4	4	8	**4**	**4/6/8**
Conversion Gain	20 dB	20 dB	16 dB	**21 dB**	**20 dB**
Noise Figure	7-8 dB	7-9 dB for 21-25GHz >10dB above 25 GHz *Q noise 3dB higher	11-13 dB	**5-9 dB**	**7 dB**
iIP3	-9.7 dBm	TBD	TBD	**est -10 to 0 dBm**	**-2 dBm**
iP_{1dB}	-16 dBm	-12 dBm	TBD	**-12 to -3 dBm**	**-12 dBm**
Power Cons. (excludes output bfrs)	185 mW	280-450 mW	280-450 mW	**110-220 mW**	**<250 mW**

2.1 Overview: Architecture, Theory, and High-Frequency Limitations

The three generations of mixer-first direct-conversion receivers share a similar architecture, as shown in Figure 3. An RF input from 10-32 GHz is directly connected to an M-phase passive mixer. A LO network creates M-phase non-overlapping clock signals. A bank of M/2 parallel baseband transimpedance amplifiers (TIAs) buffer the downconverted signals while also

providing tunable impedance matching through selectable feedback resistors. Each receiver includes a serial peripheral interface (SPI) for controlling baseband settings (not shown). The number of phases, M, is four in Gen-0 and Gen-2, whereas Gen-1 includes four-phase and eight-phase variants.

The mixer-first receiver employing passive mixers exhibits a frequency-selective impedance match around the LO frequency. In particular, the baseband termination impedance is upconverted to the LO band through the bidirectional passive mixer. By adjusting the baseband termination using the TIA feedback resistors, we can thereby tune the RF input impedance bounded by the parasitics of the mixer.

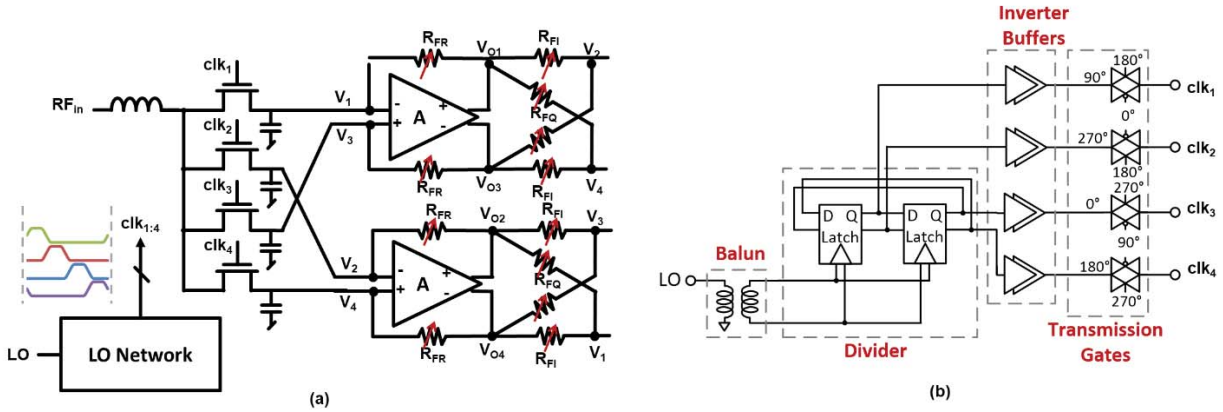


Figure 3: Block Diagram of Four-Phase Mixer First Receiver (a) and Non-overlapping LO Generation using Balun, Divide-by-Two Circuit, Buffers, and Transmission Gates (b)

As presented in Andrews and Molnar in 2010 [And10], such a mixer-first M-phase receiver provides an input impedance which is approximately by equation 1:

$$Z_{IN}(\omega) = \frac{1}{j\omega C_{in}} \left\| \left[R_{SW} + \left\{ \gamma_M Z_{BB}(\omega - \omega_o) \right\} \right\| Z_{SH}(\omega) \right]. \quad (1)$$

Here, C_{in} is the input shunt parasitic capacitance of the mixer, R_{SW} is the on-resistance of each mixer switch, and M is the number of phases. Parameter γ_M is approximately 1/M and represents the round-trip conversion loss of the mixer. Z_{BB} is the baseband load impedance of each switch and can be adjusted to alter or tune the input match of the receiver, bounded by the parasitics of the mixer. This impedance tuning can be used to compensate for parasitics at the mixer input which is the interface between the EXTENDER and CORE. For the topology shown in Figure 3(a), Z_{BB} is a closed-loop impedance given by $R_f/(1+A_{BB})$, where A_{BB} is the baseband amplifier voltage gain and R_f is the feedback resistor for the TIA. Finally, Z_{SH} is the harmonic re-radiation impedance representing the upconversion of baseband signals to frequencies around *harmonics* of the LO. For a four-phase mixer, Z_{SH} is described in equation 2:

$$Z_{SH}(\omega) \propto \left\{ 9Z_{BACK}^{*}(3\omega_o) \right\} \left\| \left\{ 25Z_{BACK}(5\omega_o) \right\} \right\| \left\{ 49Z_{BACK}^{*}(7\omega_o) \right\} \| \ldots \quad (2)$$

Here, Z_{BACK} is the impedance looking "back" from the baseband through the switch towards the RF input source, and thus depends on R_{SW}, C_{in}, and the driving point impedance of the source (such as an antenna or the prior stage's output impedance) [And10]. The "backward" harmonic impedances appear in parallel, indicating that RF power is being delivered back to the input at harmonics of the LO. Note that the presence of C_{in} tends to short out the driving point impedance of Z_{BACK} at high harmonics; thus, Z_{BACK} approaches R_{SW} for high-order harmonics. As the LO frequency becomes larger, this "shorting out" effect occurs for earlier harmonics and thus, Z_{SH} reduces. This reduction to Z_{SH} is one limitation in operating mixer-first receivers at very high frequencies.

Many researchers have demonstrated mixer-first M-phase receivers in prior work below 5 GHz. Out team at NCSU was the first to demonstrate this technique at 20-30 GHz [Wil16]. Concurrent to our publication, the Cornell team published a comprehensive theory for passive mixers and their technology and frequency limits [Yan15]. Together, these create both a theory [Yan15] and experimental demonstration [Wil16] of passive mixers operating above 20 GHz.

There are two fundamental challenges of the passive mixer operating at these higher frequencies. The first challenge is the difficulty in generating non-overlapping M-phase LO signals to drive the M mixer switches. For broadband operation, a clocking circuit is needed which can provide high rise/fall times and minimal clock overlap across a wide range. The second challenge is managing the RF parasitics at the mixer input, namely C_{in}. Although this shunt capacitance can be tuned out using an inductor for the fundamental LO frequency, this inductor has minimal effect at LO harmonics. This manifests in reduced magnitude of Z_{SH} as the LO frequency is increased, as described above. As a result, the maximum achievable input impedance is reduced at higher frequencies, compromising impedance tuning range among other things, such as filtering capability. Ultimately, this parasitic limitation is governed by the "on-off" impedance ratio of the metal-oxide semiconductor field-effect transistor (MOSFET) used to create the switch. Larger switches enable lower on-resistance but have higher shunt capacitance; smaller switches exhibit the opposite. GF's 45-nm SOI CMOS exhibits a very competitive on-off impedance ratio, given by an $R_{on}C_{off}$ time constant of approximately 125 fs in simulation for the native device and increasing to ~185 fs when including wiring parasitics to top-level metal. As we will show, this enables operation beyond 30 GHz; however, both mixer and LO network design is still difficult.

These limitations related to passive mixers at >10 GHz formed the underlying technical challenges in our receiver design work. As we will demonstrate, we investigated approaches to realize robust non-overlapping clock solutions and simple design techniques to manage input parasitics. In summary, we found that our active LO networks can work up to 33 GHz and our impedance tuning range is limited to approximately 2:1 at this upper frequency. We see LO tuning capability over 6 to 33 GHz, well-matched input impedance, and frequency-selective conversion gain with moderate linearity. The write-up below summarizes our findings for three generations of mixer-first receivers which have been demonstrated along with an alternative transconductor-first architecture with mixer-based feedback which we explored via simulation. It was not taped out due to resource constraints.

2.2 Frequency Plan Modification

During the period of performance, we revised the frequency plan to accommodate export restrictions related to 5G transceiver cores. In particular, export control restricts PA operation within 31.8-37 GHz. Note that when EPIC is used as a purely defense-based system, the 31.8-37 GHz range would be permissible; however, if EPIC is based on commercially available IP, then that IP should not support the 31.8-37 GHz range. As a result, we modified the EPIC frequency plan to accommodate this restriction and only operate up to 32 GHz. We revised the frequency range from an original plan of 24-44 GHz down to 15-32 GHz. As shown in Table 2, this range still supports broadband operation of the phased array from 15 to >200 GHz, since the IF of these systems falls within 15-32 GHz.

Table 2. Revised Frequency Plan for EPIC

X = Multiplication Ratio on EXTENDER

Fundamental Operation, Modes 1 & 2

		RF	15	30	45	60	75	90	105	120	135	150	165	180	195	210	225	240	
X	0	IF=RF	15	30	45	60	75	90	105	120	135	150	165	180	195	210	225	240	MODE 1
X	1	IF	7.5	15	22.5	30	37.5	45	52.5	60	67.5	75	82.5	90	97.5	105	112.5	120	
X	2	IF	5	10	15	20	25	30	35	40	45	50	55	60	65	70	75	80	MODE 2
X	4	IF	3	6	9	12	15	18	21	24	27	30	33	36	39	42	45	48	
X	8	IF	1.7	3.3	5	6.7	8.3	10	11.7	13.3	15	16.7	18.3	20	21.7	23.3	25	26.7	

Subharmonic Operation, Mode 3

		RF	15	30	45	60	75	90	105	120	135	150	165	180	195	210	225	240	
X	0	LO	5	10	15	20	25	30	35	40	45	50	55	60	65	70	75	80	MODE 3

Amplifier-first modes | Mixer-first modes | Both modes supported

2.3 Gen-0 Four-Phase Mixer-First Receiver

2.3.1 Gen-0 Receiver Design

Our initial receiver (Gen-0) was taped out in March 2016, prior to start of the DARPA project; however, it was measured during the first year of the EPIC program. Measurements were completed in October 2016. This design formed the starting point for our EPIC receiver design efforts.

The receiver has four phases (M=4) and follows the architecture in Figure 3 for both the receiver and LO networks. The input match includes an on-chip series inductor and transmission line (t-line) to tune out C_{in} at the LO frequency. Compared to our prior work in [Wil16], the key modification was in regards to the LO network, where a divide-by-two active LO generation scheme is used (Figure 3 (b)). Further details of the basic LO network is provided in the receiver write-up for Gen-1, in which the divider and latches were more carefully optimized. In Gen-0, the divider was a standard current-mode logic (CML) divider.

Three variants of Gen-0 were designed, as follows: Variant A uses an off-chip balun to generate differential input clock signals; variant B uses on on-chip balun tuned to 45 GHz; variant C uses an on-chip balun tuned to 54 GHz. At the time of design, we did not have a broadband on-chip

balun solution; henced, we opted for this approach using multiple design variants. Die micrographs are shown in Figure 4.

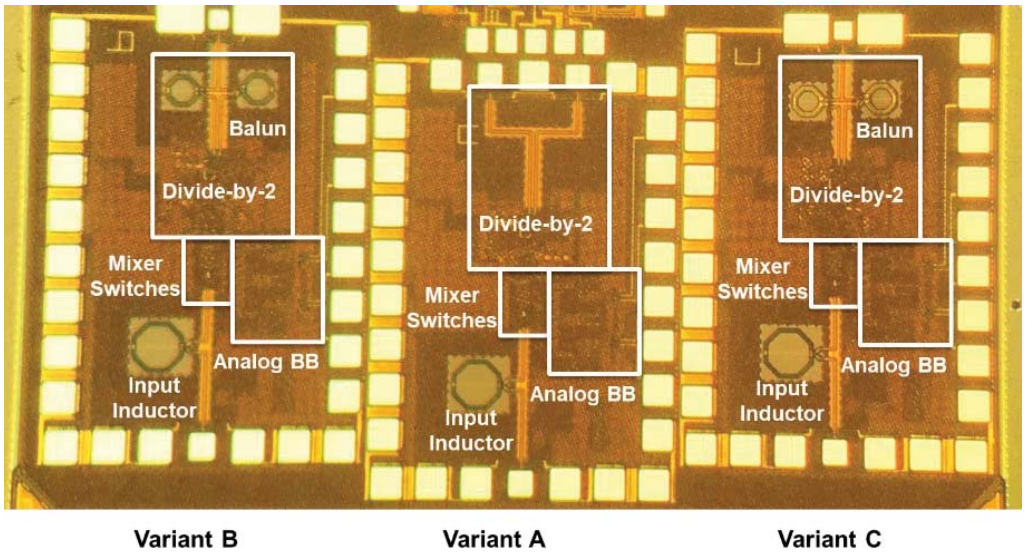


Figure 4: Die Micrographs of the three Variants of the Gen-0 Receiver

2.3.2 Gen-0 Measurement Results

The three Gen-0 receiver variants were characterized through measuring double-sideband noise figure (NF_{dsb}), input one-dB compression point (iP_{1dB}) and conversion gain via wafer-level probing. For these measurements, we plot the in-band conversion gain, NF_{dsb}, and iP_{1dB}, as LO frequency is swept across its full range. Figure 5 shows the measured results of the Gen-0 receiver compared to the results we demonstrated previously in [Wil16]. For any one LO frequency, we see a frequency selective gain and noise response, similar to that shown in Figure 6 for [Wil16]. As can be seen in Figure 5, the peak performance across the band is flat proving that clocking is the major bottleneck in achieving extremely wideband receivers. Also, as evident from the fact that there were three variants, a broadband balun is also required for broadband mixer-first receiver operation.

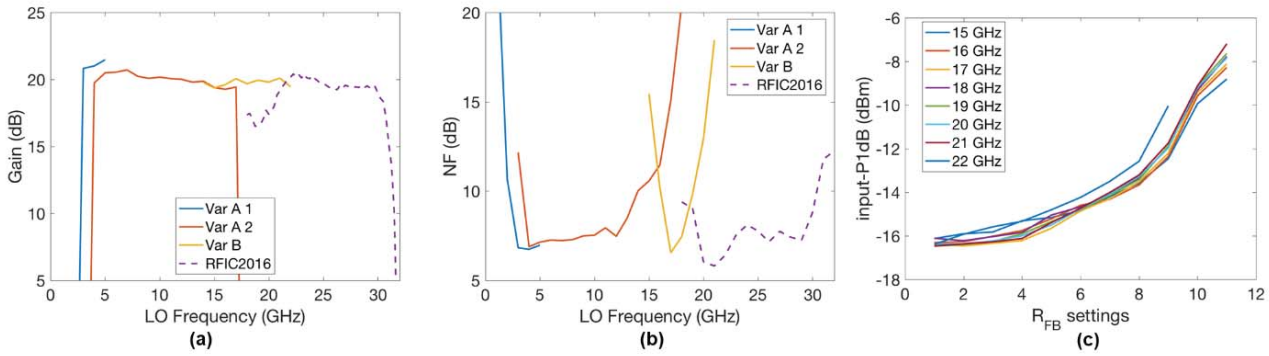


Figure 5: Measurement Results for Gen-0

(a) Conv. gain vs. frequency, (b) minimum achievable NF across baseband vs. corresponding RF frequency for finite R_{FR}, and (c) input P1dB at 10 MHz offset from the LO.

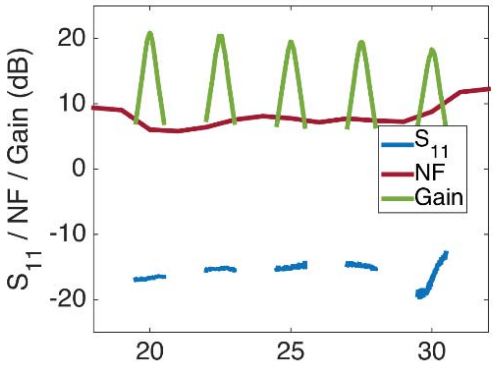


Figure 6: Measurement Results of Mixer-First Receiver at five different LO Frequencies [Wils16], Illustrating Selectivity

In our Gen-0 measurements, we present two different operating points for variant A (using off-chip clock balun), where the bias level within the LO frequency divider was adjusted to allow operation to lower frequencies, labeled Var A1 and Var A2 in Figure 5. Also, we see that variant B (on-chip 45 GHz balun) exhibited a very narrow operational range. Finally, variant C (on-chip 54 GHz balun) did not function and is not included within any plots. We also observe that the Gen-0 receiver can only operate up to about 20 GHz, whereas our prior work in [Wil16] which employed a passive four-phase clock generation network can operate up to 30 GHz. From this, we conclude that the primary limitation in Gen-0 was four-phase clock generation, where this particular low-power divide-by-two circuit did not operate above 40 GHz.

The RF performance of this receiver is summarized as follows. Conversion gain across 2.5-20 GHz is approximately constant at 20 dB. NF_{dsb} can reach a minimum value of around 7 dB, though there is sharp increase in NF outside of the LO "sweet spot". This indicates that the LO divider output swing quickly degrades outside of its intended range. Finally, iP_{1dB} is -16 dBm at maximum gain setting (R_{FR} setting 1) and increases to -8 dBm at minimum gain setting (R_{FR} setting 11). The receiver's compression is limited at the baseband amplifier output, which is the first point where significant voltage swing is encoutered. Put another way, for all gain settings, the output compression voltage of the receiver is approximately +4 dBV, differential.

We characterized the Gen-0 receiver (Var-B) input impedance tuning by measuring the input reflection coefficient (S_{11}) at select LO frequencies. Figure 7 shows the input reflection at two different frequencies where the TIA feedback resistors are tuned across all possible values. Note that our receiver includes two types of feedback for tuning impedance. We have "within-phase" feedback between a given TIA's output and input using R_{FR} from Figure 3(a). This allows tuning of the real-part of impedance. There is also "quadrature-phase" feedback between a given TIA's output and adjacent TIA inputs which are 90 degree offset, using $R_{FI/Q}$. This "IQ" feedback provides a way to introduce an active (or closed loop) susceptance for input matching.

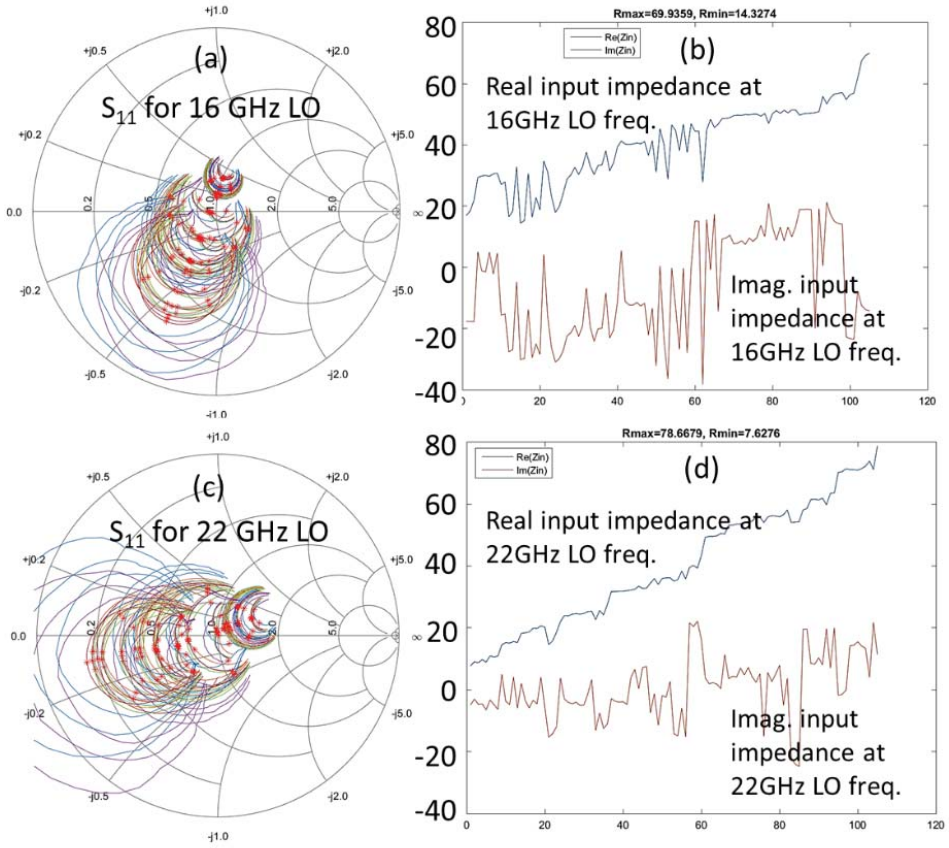


Figure 7: Gen-0 Measured Input Reflection Coefficient (S11) at RF Port when Baseband Impedances are Swept (a), (c) and Measured Real and Imaginary Input Impedance Values vs. Baseband Impedance Setting (b), (d)

Figure 7(a) shows S_{11} on a Smith Chart with LO frequency set to 16 GHz. The red dots correspond to the S_{11} at the LO frequency of the mixer, where the curves themselves represent the performance across frequency (i.e., swept RF with fixed LO). From this result, we see that the receiver can be well-matched at the LO frequency (i.e., the red point can be located at the center). We also see the impedance tuning range in terms of the range or distribution of those red points on the chart. This is further illustrated in Figure 7(b) which plots the real and imaginary parts of the impedance as a function of digital-to-analog converter (DAC) setting. Approximately a 3:1 ratio can be achieved for tuning of the real part whereas tuning of the imaginary impedance is more restricted due to a design error within the Gen-0 quadrature resistor coupling network. Finally, note that some resistor values which couple stronger out-of-phase signals result in negative active resistance and this results in terminations outside the Smith chart in a predictable way. These settings are to be avoided during operation.

Figure 7(c) and 7(d) show the results for a 22 GHz LO frequency. We observe similar results except that the locus of points on the Smith Chart has rotated clockwise as expected due to the presence of the series t-line and inductor on the receiver input. Once again, very good input match can be achieved at 22 GHz.

Given the limited frequency range for all three variants, we worked to understand the limitations in our LO network, as we needed to fix these in the Gen-1 receiver. Unfortunately there was no stand-alone break-out of the clock generation circuit or frequency divider; hence, we relied on a combination of receiver measurement and divider simultions. This debugging suggested two reasons for the degraded performance. First, the internal input bias of the inverter-based buffer was set at $V_{dd}/2$ through a resistive divider. This was not the optimum bias point, as it reduces the transonductance and reduces the maximum operational frequency. Second, we found that the supply distribution to the inverter based buffer had a voltage drop due to high supply-line resistance. This translated to amplitude and phase mismatch across the four phases.

In summary, the key take-away from Gen-0 measurements are that acceptable broadband RF performance can be achieved in four-phase mixer-first receivers in 45nm SOI CMOS; however, the LO network is the key limiter for achieving higher frequency operation. As a result, our Gen-1 design efforts focused considerably on LO network optimization. We also saw that the linearity of the receiver was limited by the baseband amplifier; hence, in Gen-1 we worked to enhance the dynamic range of that amplifier and increase its bandwidth.

2.4 Gen-1 Four-Phase and Eight-Phase Mixer-First Receivers

2.4.1 Gen-1 Receiver Design

Gen-1 receivers were taped out in April 2017 and most measurements were completed by January 2018. Two versions were taped out - one which employs four phases and another which employs eight phases. The Gen-1 receiver tape-out was initially planned for November 2016 for a single, reconfigurable 4/6/8 mixer-first receiver. To include the inferences from the Gen-0 measurements completed in October 2016 and due to the extensive design improvements, the tape out was shifted to the March 2017 run.

In the tape-out of Gen-1, we faced numerous challenges over and above the expected technical ones. In particular, in early 2017, GF made a significant update to their design kits for 45-nm RFSOI. This update introduced mm-wave enablement, such as transmission lines and better RF field-effect transistor (FET) models; however, the new design kit had many bugs which required significant effort to report to GF and/or manually fix ourselves. This included having to write custom scripts to allow us to port our designs from the prior kit to the new kit, custom approaches to handle bugs in the parasitic capacitance extraction (we were seeing random nanoFarad capacitors pop up in our netlists), and many other problems. Altogether, this resulted in over four weeks of additional work in porting our designs and dealing with the new design kit. We were still able to make the tape-out, which GF postponed to April 10, 2017 due to the problems with the kit which affected all customers; however, we did have to relax a design goal for the RX from a single selectable four/six/eight-phase design, to separate four and eight-phase designs.

The four-phase Gen-1 receiver follows the same architecture as shown in Figure 3, and shown again in Figure 8 along with a layout view of the circuit. The four-phase mixer-first receivers targeted 22-44 GHz operation. Compared to Gen-0, key changes were made to the TIA to improve dynamic range and the LO network to enhance frequency range. Note that the LO

network now includes a frequency doubler before the divider allowing use of lower frequency input clock signals.

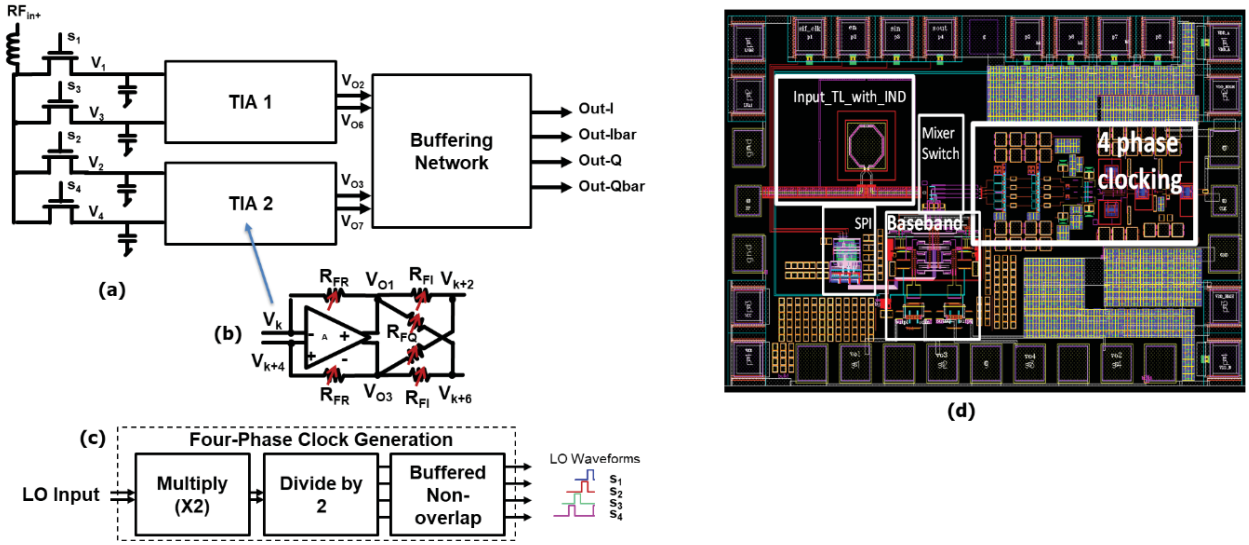


Figure 8: Diagrams of Four-Phase Gen-1 Receiver (a), TIA (b), LO Network (c), and Screenshot of Layout (d) all in 45-nm SOI CMOS

The eight-phase Gen-1 receiver employs the architecture shown in Figure 9. The eight-phase mixer-first receivers targeted 11-22 GHz operation which is half the frequency of the four-phase system. This relationship comes from the minimum achievable pulse width in the LO network which corresponds to 44 GHz operation for four-phase non overlapping clocks and 22 GHz for eight-phase non overlapping clocks. The TIA is identical to that for the four-phase receiver. The LO network includes the same doubler but now a divide-by-four circuit for generation of eight-phase clocks.

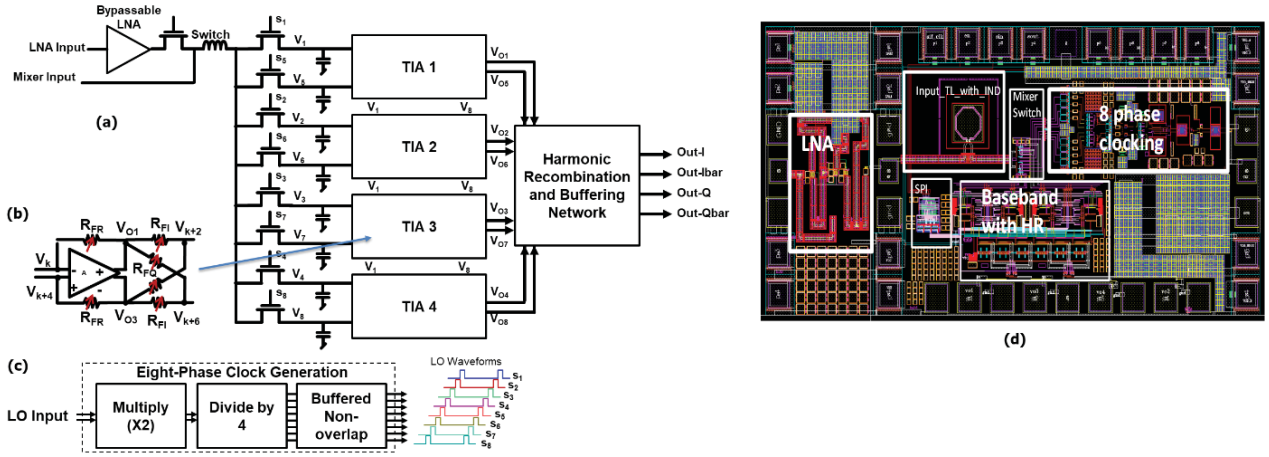


Figure 9: Diagrams of Eight-Phase Gen-1 Receiver (a), TIA (b), LO Network (c), and Screenshot of Layout (d) all in 45-nm SOI CMOS

A 20-44 GHz bypassable LNA was included in front of the eight-phase mixer. This LNA can be switched out of the circuit and a separate RF input pad is used when direct connection to the mixer is desired. Note that the LNA was designed to improve noise figure for 20-44 GHz. As such it could have been inserted in front of the four-phase mixer-first receiver; however, we opted not to do so to allow us to evaluate the best possible performance for the stand-alone four-phase receiver. Instead, we included this LNA as a separate breakout and then integrated it with the eight-phase receiver. It would be used when that receiver is operated in a third-harmonic mode. In hindsight, this may have been a poor choice and the LNA would have been better placed in front of the four-phase receiver. We therefore combine the measurements of the LNA breakout and four-phase receiver breakout to estimate cascaded performance.

2.4.2 Gen-1 LO Network Design

2.4.2.1 Four-Phase RX

The LO network for either receiver begins with a frequency doubler, shown in Figure 10(a). This doubler includes a balun for differential signal generation, a push-push circuit for doubling, a cascode amplifier, and then another balun. The same transformer was used at the input and output of divider by tuning the operating range with capacitors. The simulated bandwidth of the doubler structure was ~50-80 GHz (output referred) with the passive transformers being the bandwidth limiter. The LO network can still be operated below this frequency range by increasing the power consumption to overcome internal losses.

Following the balun, a CML based 2:1 frequency divider (Figure 10(b)) was used to generate the in-phase (I) and quadrature (Q) signals. Since the divider is a differential design, this block generated four 50% duty cycle signal with 90^0 phase shifts. Inductive peaking was used to improve bandwidth at the expense of introducing a lower frequency limitation. The divider requires at least 400mVpp clock signal at the extreme frequencies for proper operation. The input differential generation could provide this only from 50-80 GHz in simulation under normal operating conditions.

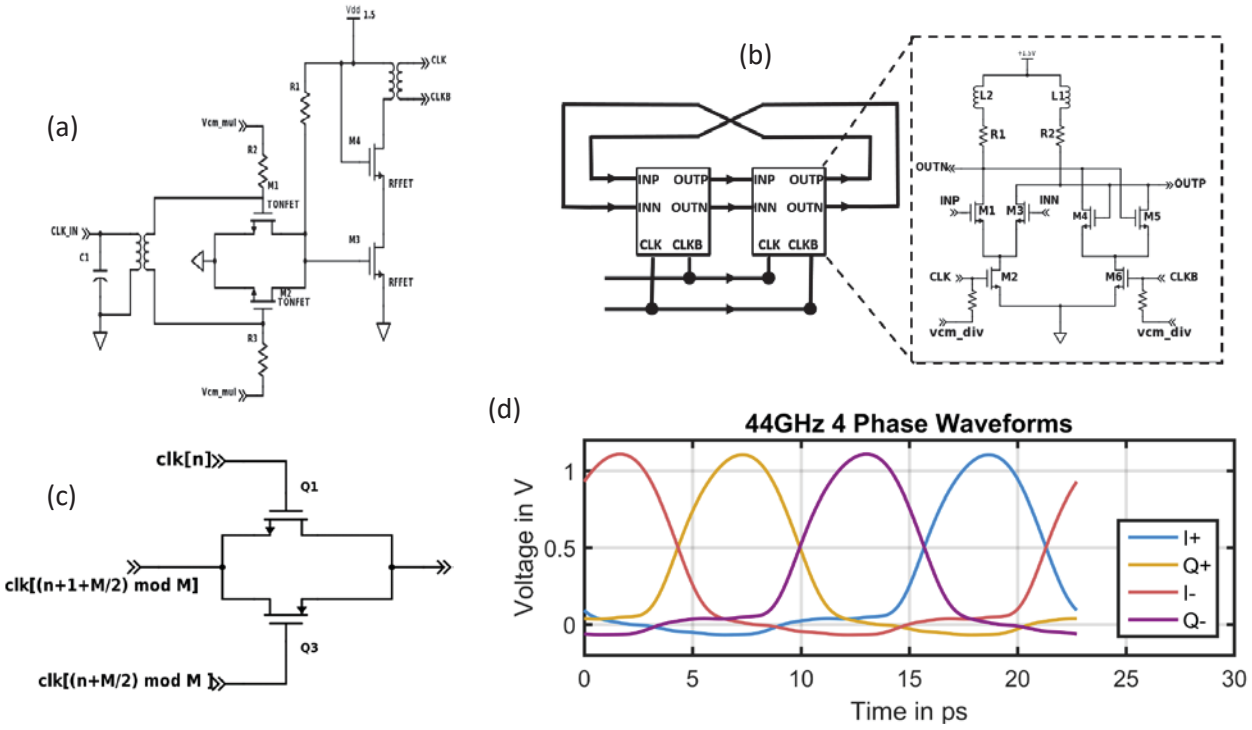


Figure 10: Frequency Doubler Schematic (a), CML Divider Schematic (b), Non-Overlapping Transmission Gate (M=4/8, n=0 to M-1) (c), and Simulated Four-Phase Non-Overlapping Waveforms at 44 GHz (d)

Following the divider is a cascade of buffers which are necessary to amplify, distribute, and repeat the signals as they are routed between the divider and the mixer. These buffers include both resistive-feedback inverter structures as well as a common-source amplifier structure. The resistive feedback inverters reduce the direct current (DC) drift across the buffer keeping the entire buffer chain at optimum bias. Total power consumption of the buffers is ~300 mW at 40 GHz. These circuits by far consume the most power within the receiver, due to the need for rail-to-rail operation for parallel cascaded buffers.

2.4.2.2 Eight-Phase RX

In the eight-phase receiver the same frequency doubler stage and divide-by-two circuit are used. Following this divide-by-two, an additional pair of static divide-by-two circuits are included, as shown in Figure 11(a). These are clocked using the in-phase and quadrature-phase outputs from the preceding divider. As such, these two circuits generate eight-phase signals at 50% duty cycle. Buffers were added before and after the static divider for proper amplification and division. The static divider uses a modified D-latch and was employed for lower power (<3 mW) and smaller area.

The 50% duty cycle waveforms in both four-phase and eight-phase generation was passed through transmission gates based circuits (Figure 10(c)) to convert these waveforms into 25% duty cycle and 12.5% duty cycle non-overlapping waveforms respectively as in Figure 10(d) and Figure 11(b).

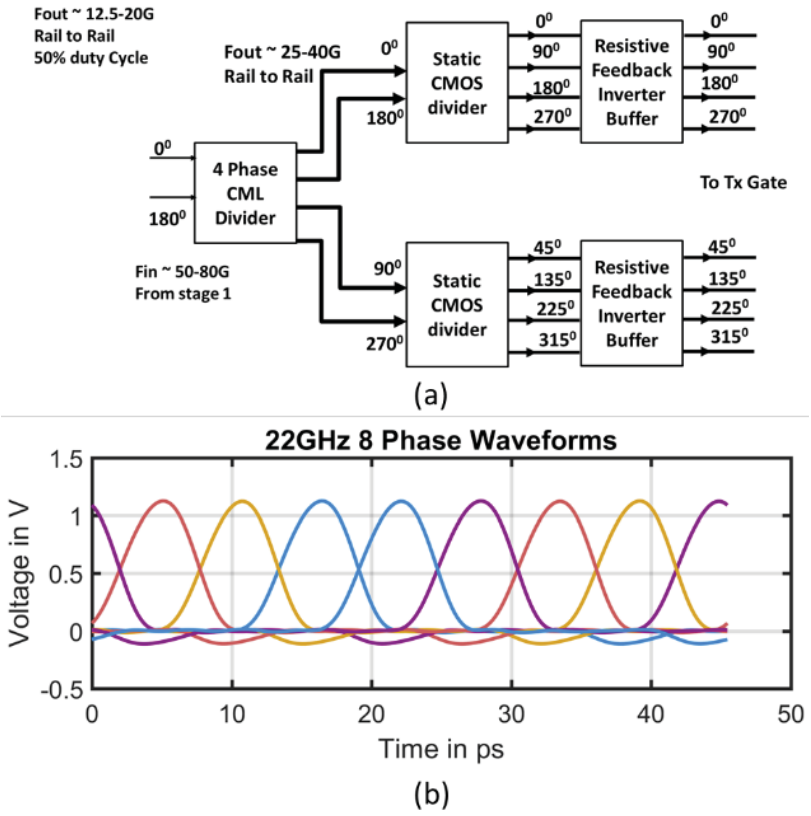
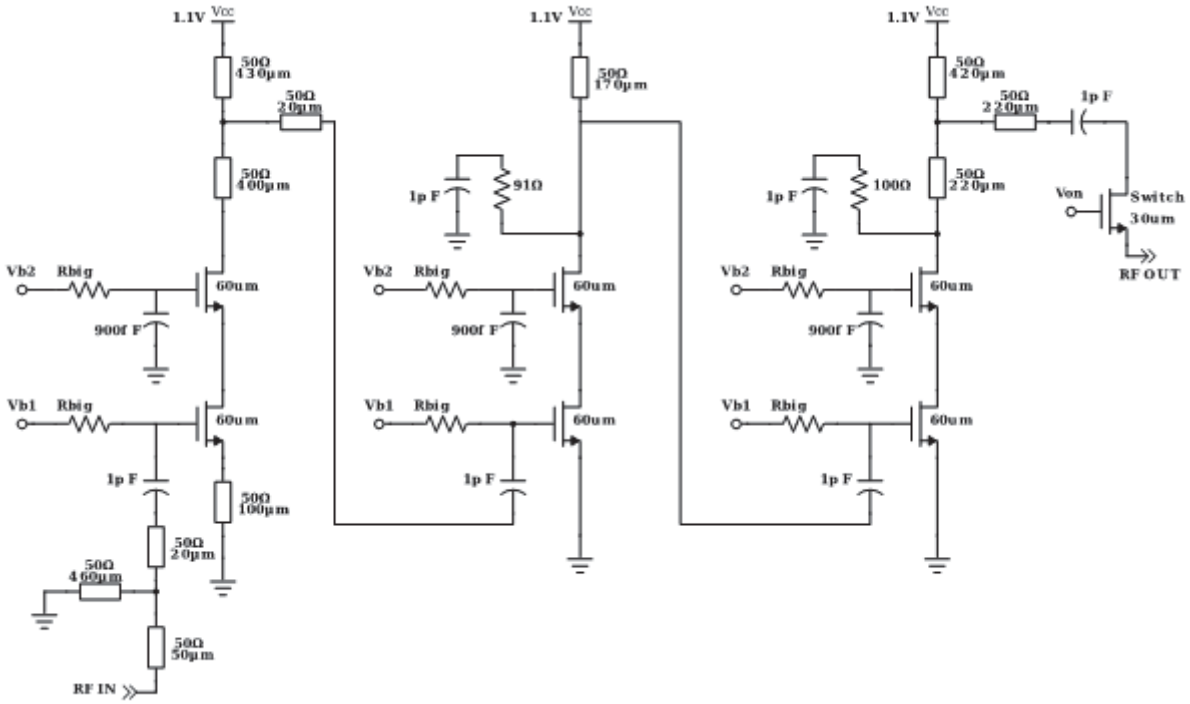


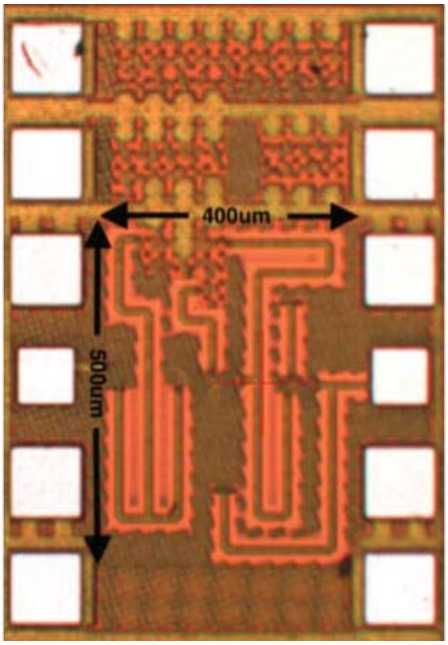
Figure 11: Eight-Phase LO Generation Block Diagram (a) and Simulated Non-Overlapping Waveforms after Eight-Phase Generation (b)

2.4.3 Gen-1 LNA Design

The LNA was designed to achieve flat gain of >18 dB gain across 24 to 44 GHz with less than 1 dB gain ripple, NF less than 5.2 dB, and iP_{1dB} of -22 dBm or better. A schematic of the LNA is shown in Figure 12(a) and a die micrograph in Figure 12(b). A three-stage design is used, with staggered frequency tuning to achieve broadband operation. The LNA employs microstrip transmission lines and metal-insulator-metal (MIM) vertically natural capacitors (VNCAPs) for all matching networks. Transmission lines are based on custom electromagnetic (EM) models validated with prior measurement. Bypassing of the LNA is achieved through inclusion of a simple series MOSFET switch at the output. When the receiver is to be operated in mixer-first mode, this switch is opened, disconnecting the LNA impedance from the mixer. Then the mixer can be driven directly using another set of pads.



(a)

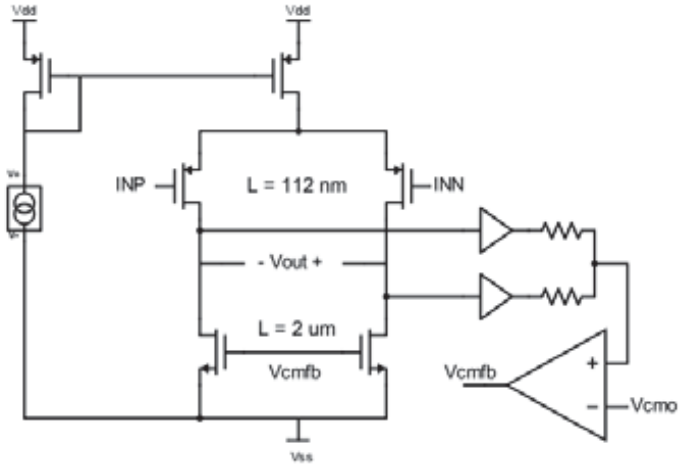


(b)

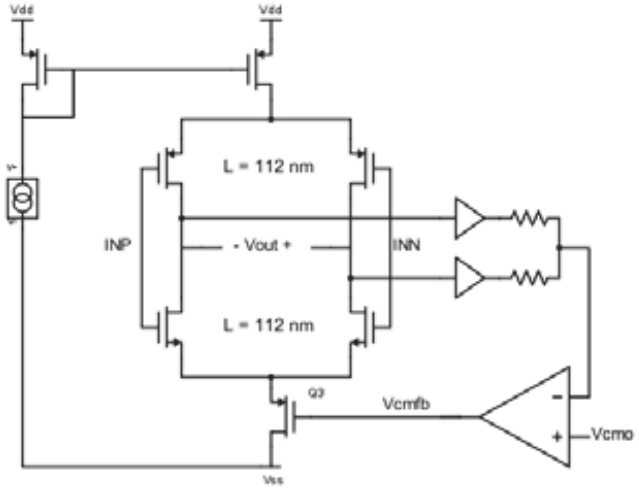
Figure 12: Schematic (a) and Die Micrograph (b) of 20-44 GHz LNA
(Active area is 400X500um^2)

2.4.4 Analog Baseband Design

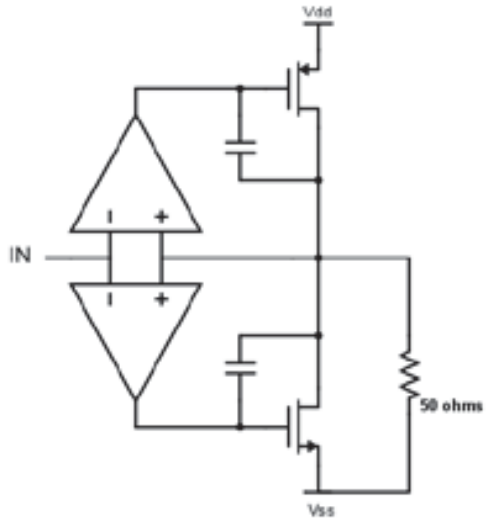
The baseband (BB) TIAs have been designed to achieve higher bandwidth, lower NF, and improved linearity at the increased power consumption level in comparison to Gen-0. The current consumption has been increased to improve bandwidth, improve driving capability of the TIA, and especially, to decrease noise. A comparison between the previous (Gen-0) and the new (Gen-1) BB amplifier is shown in Figure 13(a) and 13(b). The Gen-1 baseband switched to complimentary transconductance for increased gain and reduced noise. Finally, the output of the BB amplifier is fed to a newly designed driver stage which employs a gain-boosted complimentary buffer topology, as shown in Figure 13(c). Compared to our prior version, the new baseband amplifier achieves similar gain (~16 dB) but 5X improved bandwidth, where the 0.8-dB BW is 2.1 GHz in simulation. Also, the input-referred noise floor is ~0.6 nV/rt(Hz), which is reduced by 3X compared to the prior version.



(a)



(b)



(c)

Figure 13: Schematic of old BB Amplifier (a), Schematic of new BB Amplifier (b), Schematic of new Output Buffer (c)

For the eight-phase system, a harmonic recombination network is used to weight and combine BB phases such that the downconverted response around the first harmonic of the LO is maintained but the response around third and fifth are cancelled. A voltage-mode topology is used based on simple weighted resistors. This voltage mode circuit requires strong output buffers but works well when driving 50-Ω outputs.

2.4.5 Gen-1 Measurement Results

2.4.5.1 Four-Phase Results

The four-phase receiver was characterized through measuring input impedance, NF_{dsb}, P_{1dB} and conversion gain across LO frequency and feedback resistor (or gain) settings.

Figure 14(a) shows the conversion gain for LO frequencies swept from 20 to 38 GHz in 1 GHz steps while RF frequency is swept +/- 500 MHz. For each LO frequency, we include multiple gain plots corresponding to various feedback resistance settings. Note that these curves show high frequency selectivity which is not caused by our on-chip baseband but is instead limited by an off-chip, board-level transformer in our setup. These data show that LO network functions across 21 to 38 GHz; however, the mixer becomes starved for LO around 31 GHz.

Figure 14(b) shows the measured iP_{1dB} versus LO frequency for multiple feedback settings. Once again, this design's linearity is limited by the baseband amplifier output node.

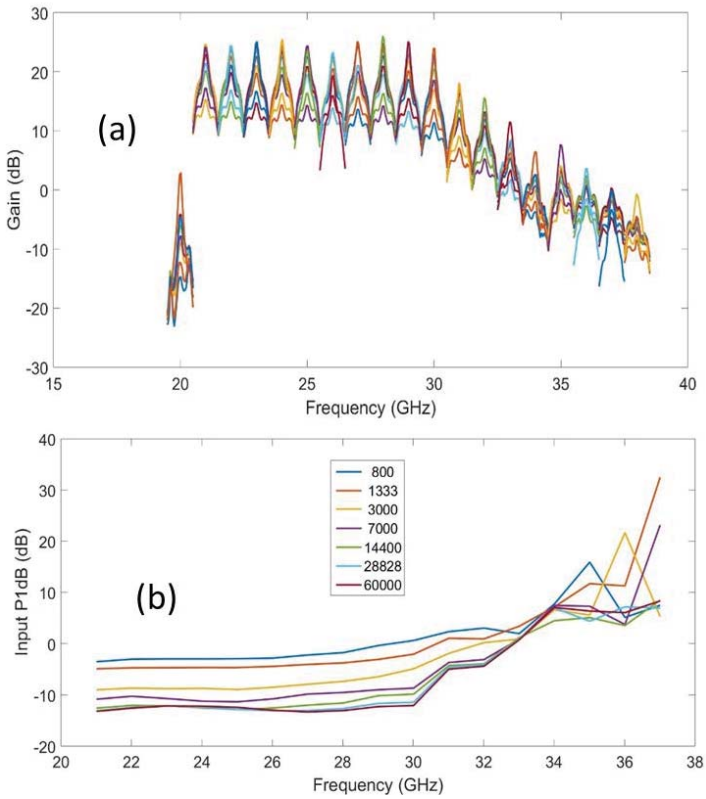


Figure 14: Measured Gen-1 Conversion Gain (a) and iP_{1dB} vs. LO Frequency for Multiple Gain Settings (b)

Figure 15 shows the NF for I channel measured across frequency for each feedback resistance. A 7 dB NF is achieved around 22 GHz; however, it increases outside of the 20-24 GHz range. Furthermore, the results are shown only up to 25 GHz since NF exceeds 10 dB above that frequency and our spectrum analyzer noise measurement is inaccurate when NF exceeds this level. As in Gen-0, the poor NF performance outside of this frequency range is attributed to poor LO drive. We also observed higher NF in the Q channel.

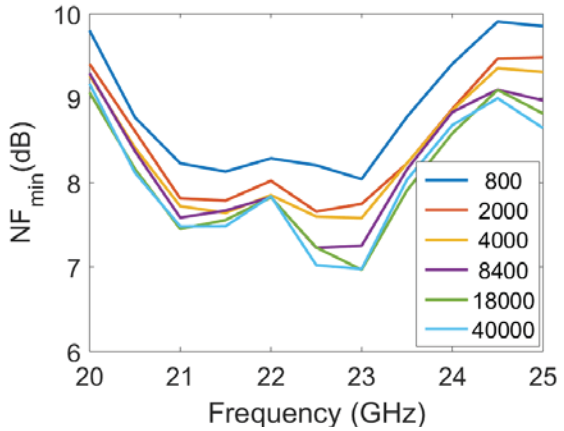


Figure 15: Measured Gen-1 NF_{dsb} across Frequency as Feedback Resistance is increased from 800-60K

Figure 16 shows the measured conversion gain and noise figure for both I and Q channels at 23 GHz as baseband feedback resistance is varied. We observe 3 dB higher NF in the Q channel as compared to I channel, although we see similar gains for both. The cause of this difference is attributed again to the LO buffers for the Q channel seeing less local supply voltage than for the I channel. Once again, we see that the key limitation in the high-frequency operation of our mixer-first receiver is achieving consistent, wideband LO drive. In analyzing our designs, we believe we were still too aggressive in minimizing power consumption and did not include strong enough buffering. Furthermore, our LO divider chain was very sensitive to parasitics and tedious to optimize. Together, these led to reduced capabilities in Gen-0 and -1.

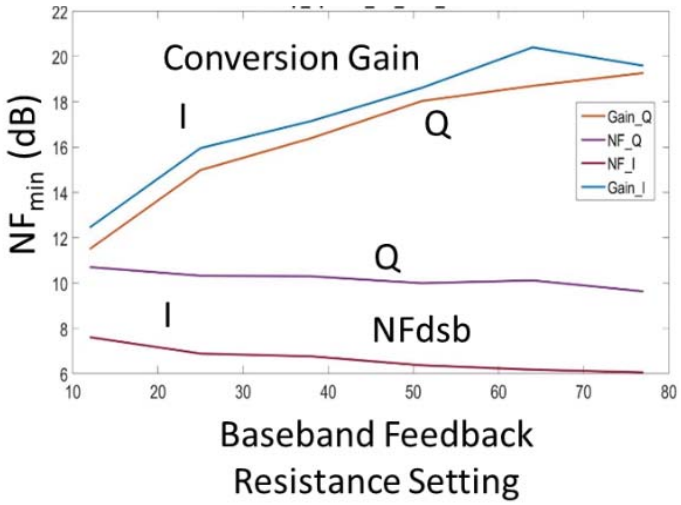


Figure 16: Measured Gen-1 Conversion Gain and NF at 23 GHz vs. Feedback Resistance Setting

Finally, Figure 17 shows the impedance tuning range through reflection coefficient (S_{11}) at two frequencies across various baseband settings including complex coupling. We observe that the overall impedance tuning range has shrunk when compared to Gen-0. This is due to a change to the mixer common-mode bias setting which impacts R_{sw} and Z_{SH}. Regardless, excellent input matching can be achieved with the Gen-1 receiver.

Power consumption of the Gen-1 receiver was 280 mW at 20.5 GHz LO and 450 mW at 33 GHz LO. Another 200 mW of power is consumed in the baseband output buffers used to drive 50 Ω loads. These are only present for test and would not be needed in a normal system.

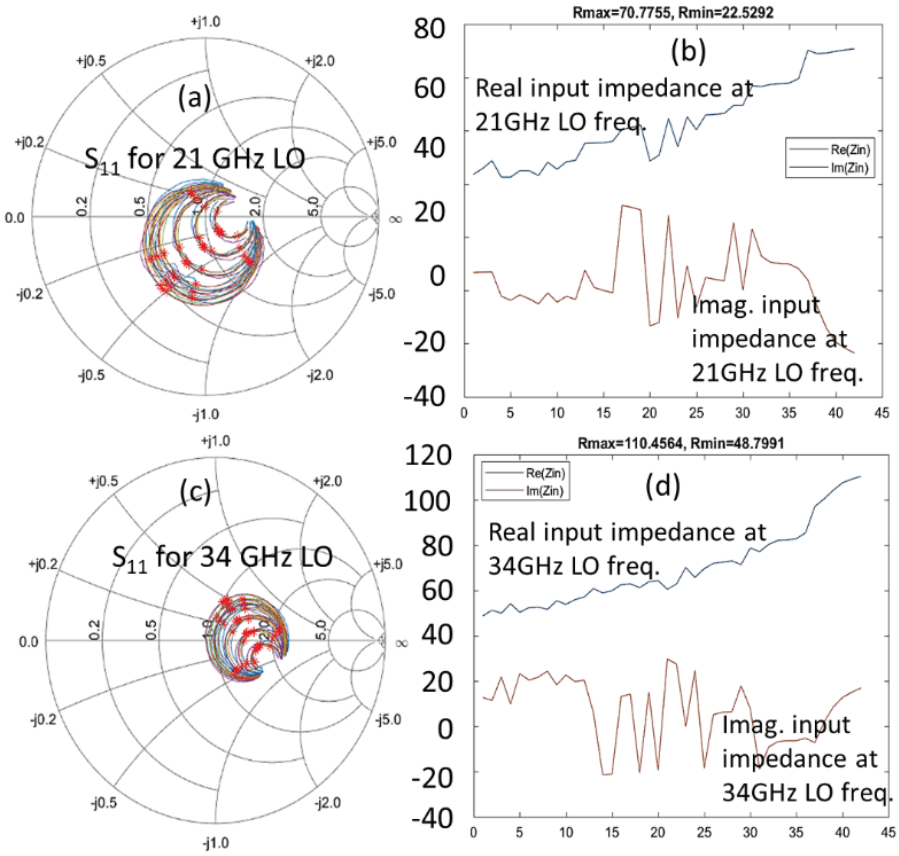


Figure 17: Gen-1 Measured Input Reflection Coefficient (S_{11}) at RF Port in (a); when BB Impedances are swept (c); Measured Real and Imaginary Input Impedance Values in (b); and (d) vs. BB Impedance Setting

2.4.5.2 Eight-Phase Results (LNA bypassed)

The eight-phase receiver was characterized through NF_{dsb} and conversion gain. The input impedance and linearity of the eight-phase receiver was not measured due to a short-term equipment shortage. They were then deferred until after the Gen-2 tape-out and measurements. They will be completed in the coming months.

Unfortunately, our LO network for the eight-phase receiver had a phase ambiguity. In particular, as shown in Figure 11(a) the final two parallel divider in eight-phase receiver are asynchronous and can lock on to either I+(Q+) or I-(Q-) signals. Due to the operation of the transmission gates for generating final output signals, if the divider locks on to the wrong signal, instead of 12.5% duty cycle non-overlapping signals, the transmission gate generates overlapping 87.5% signals. We therefore had to manually check that the dividers were properly locked, and our automated measurement scripts could not be used.

The eight-phase receiver was verified to work over ~10.5 -16 GHz. Based on the four-phase receiver result above (which worked from 21-38 GHz), we would expect the eight-phase receiver to work across 10.5 to 19 GHz. Our measurements indicate a slightly lower maximum frequency. *It should be noted that this 10 to 16 GHz operation is the highest eight-phase demonstration to date to our knowledge*.

Figure 18 shows the NF and conversion gain at NF for the eight-phase receiver in fundamental mode. These measurements show that the eight-phase mixer-first receiver can achieve 11-13 dB NF and 8-16 dB conversion gain. Compared to the four-phase receiver, this eight-phase design shows 3-5 dB worse NF. This is in contrast to lower frequency M-phase mixers, where the eight-phase mixer shows better NF than a four-phase counterpart. *From this data, we conclude that there does not seem to be any benefit to using eight phases at this time when operating near technology limits for the passive mixer. A four-phase design exhibits higher frequency, lower noise figure, and simpler LO network design.*

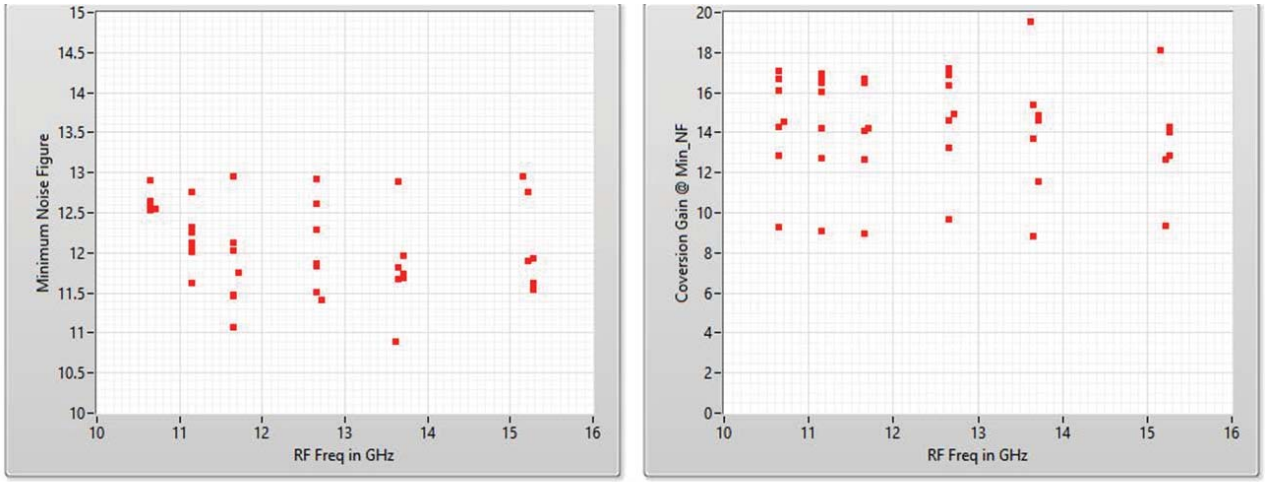


Figure 18: Measured Gen-1 Eight-Phase Receiver NF and corresponding Conversion Gain in Fundamental Mixing Mode

*RFin = 0.5*FLO+BB. Here the input LNA is bypassed*

2.4.5.3 LNA Measurement Results

The stand-alone LNA circuit was characterized through wafer probing. Supply voltage was 1.1V and supply current was 52mA. Figure 19 shows the measured and simulated S-parameters results from 20-50 GHz. The measured S_{21} agrees the simulation except for a 4-GHz frequency shift of the first stage resonance from 24 to 28 GHz. The gain peaks at 20 dB at 28 GHz with a 3-dB band-width from 24-47.5 GHz (65%). There is a similar frequency shift in the input matching; S_{11} is above -10 dB for 24-27 GHz and under -10 dB from 27-48 GHz (the desired range). The output return loss is greater than 10 dB for the entire frequency band and up to 67 GHz. The measured S_{12} is <-45 dB up to 44 GHz.

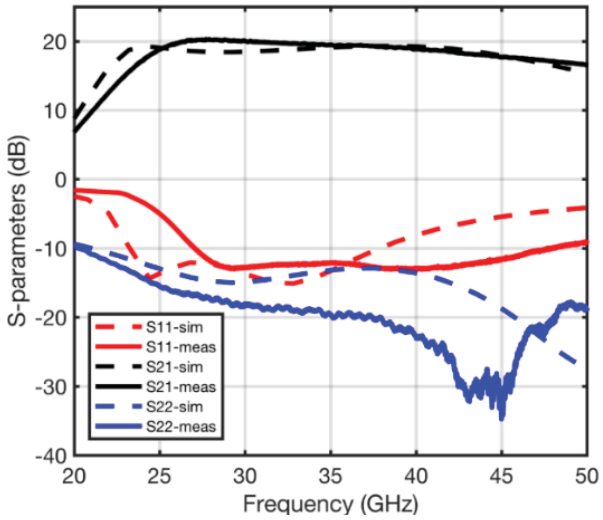


Figure 19: Measured vs. Simulated S-parameters of LNA

The NF is measured using the Y-factor method. Results from five different readings and an average of these readings are shown in Figure 20 along with the simulated NF. The noise figure is 4-5.5 dB in the 24-44 GHz range. The measured input P_{1dB} is -17 dBm at 24 GHz, -19 dBm at 28 GHz and -16 dBm at 39 GHz. These LNA results were published in the 2018 Institute of Electrical and Electronics Engineers (IEEE) Global Symposium on Millimeter Waves (GSMM) [Cha18].

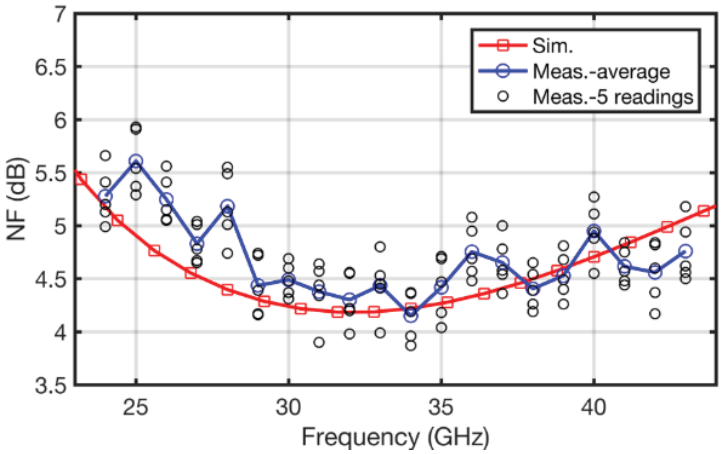


Figure 20: Measured vs. Simulated Noise Figure of LNA

2.4.5.4 Subharmonic Eight-Phase Measurement Results with LNA enabled

Figure 21 shows the NF and conversion gain for the LNA+eight-phase receiver with mixer in subharmonic mode (RF is at the third harmonic of the LO). Measured NF is between 6 and 12 dB, with an average value of 9 dB. Given that the LNA NF is 5 dB and gain is 20 dB, this indicates that the NF of the subharmonic mixer is larger than 20 dB which is higher than simulation by approximately 8 dB. We are still unsure of the reason of this much higher NF in subharmonic mode. We hypothesize that it is again due to LO signals with slower rise/fall times and thus less harmonic content. *From this result, we conclude that operating the receiver in a third-harmonic mode is not useful for the overall EPIC system.*

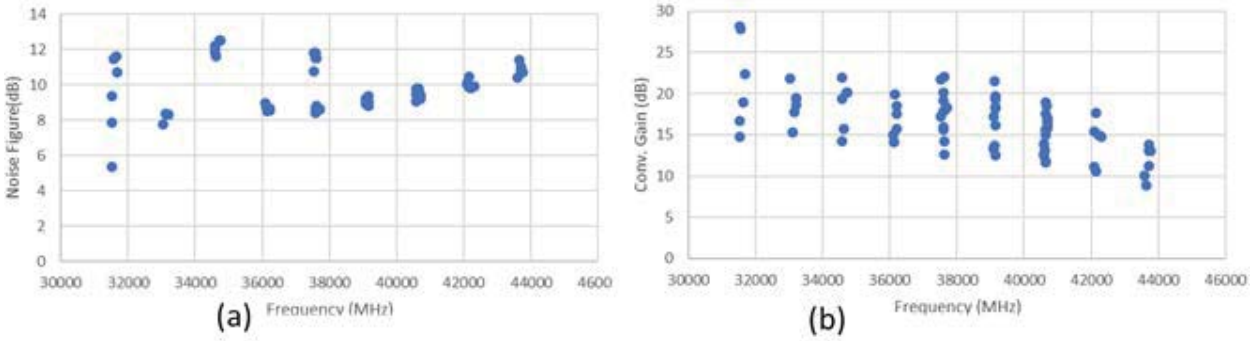


Figure 21: Measured Gen-1 Eight-Phase Receiver NF and corresponding Conversion Gain in Subharmonic Mixing Mode with LNA enabled
*RFin = 1.5*FLO+BB.*

2.4.6 Estimation of LNA plus Four-Phase Receiver

As mentioned earlier, we did not include a hardware variant which included the broadband LNA and the four-phase receiver. We therefore estimate its performance based on cascading the measured performance numerically. The broadband LNA achieved 5 dB NF, 20 dB gain, and -16 dBm iP_{1dB} for 24-44 GHz. The four-phase mixer-first receiver achieved 6-8 dB NF, 10-20 dB gain, and -12 to -3 dBm iP_{1dB} for 6-33 GHz. A cascaded LNA plus four-phase mixer would therefore have 5.1 dB NF, 30-40 dB gain, and -32 to -23 dBm iP_{1dB}. Although this shows improved NF over a mixer-first receiver, we see that the linearity is significantly degraded due to the presence of the multi-stage LNA. *As a result, the mixer-first receiver appears to be the preferred solution for wideband systems which require high dynamic range*.

2.4.7 Debugging of LO Network Based on Gen-1 Measurement Results

To summarize, from the above, we see that our Gen-1 four-phase receiver had an upper frequency limit of ~25 GHz (as compared to 40 GHz in simulation) and 3 dB higher NF in Q channel compared with I channel. Also, our Gen-1 eight-phase receiver in subharmonic mode exhibited much higher NF than expected. We therefore continued to investigate our LO network to understand its limitations.

Our investigation pointed to an error in the model of our custom transformer and how the center-tap was being used within the layout. As described in our quarter-6 report, we saw mismatch

between our measurement of the transformer test structure and our EM model (from Momentum). In particular, our model was not correctly capturing the common-mode signals which flow through the center tap. When this transformer is used within large-signal circuit such as a doubler, there is significant common-mode signals. Once we discovered this error, we went back and revised the model and re-simulated the overall LO network. From this we saw that the frequency range of the overall LO network reduced from 25-40 GHz to 20-32 GHz. This is in agreement with the Gen-1 measurements. This issue was fixed in Gen-2.

2.5 Gen-2 Four-Phase Mixer First Receiver

2.5.1 Gen-2 Receiver Design

A final generation of the receiver was taped out in February 2018 with key measurements completed by August 2018. The receiver features the same architecture as shown in Figure 8 with a revised LO network. As argued above, the Gen-2 receiver only focused on a four-phase variant, since eight-phase showed poor performance. Furthermore, as just discussed, the utility of the LNA with a properly working four-phase passive mixer is debatable, since the LNA NF is 5 dB whereas the mixer NF is 6-8 dB. This 1-3 dB improvement in NF comes at 9-20 dB degradation to iP_{1dB}. We therefore opted to eliminate the LNA.

For Gen-2, as in Gen-1, we encountered additional tape-out challenges. MOSIS and GlobalFoundries changed the required metal stack-up for 45RFSOI technology from an 11-metal stack to an 8-metal stack. Also, the top-level metals were of different DRC rules, preventing any automatic translation of layouts. As a result, all the commonly used cells and entire Gen-1 four-phase receiver had to be first translated to the new stack. Custom inductors used in Gen-1 had to be replaced with kit inductors with different metal properties. Altogether, this led to approximately three-week delay (**Note that it appears that GF has settled down to a stable version of 45RFSOI in the last six months).

A block diagram of the revised LO network for Gen-2 is shown in Figure 22(a). First, the input frequency doubler was removed to mitigate risk and provide the ability to overdrive the input signal to the divider if needed. Moreover, the lower frequency limit in Gen-1 was due to the doubler; hence, Gen-2 could operate to lower frequencies if the doubler was removed. Second, the transformer balun's center tap was fixed, showing correct performance up to 70 GHz (corresponding to 35 GHz LO signals for the mixer). Operating above 70 GHz would require an additional amplifier; hence, we opted to target the Gen-2 LO for 10-35 GHz which is consistent with our modified frequency plan. Figure 22(b) shows the Gen-2 die photo.

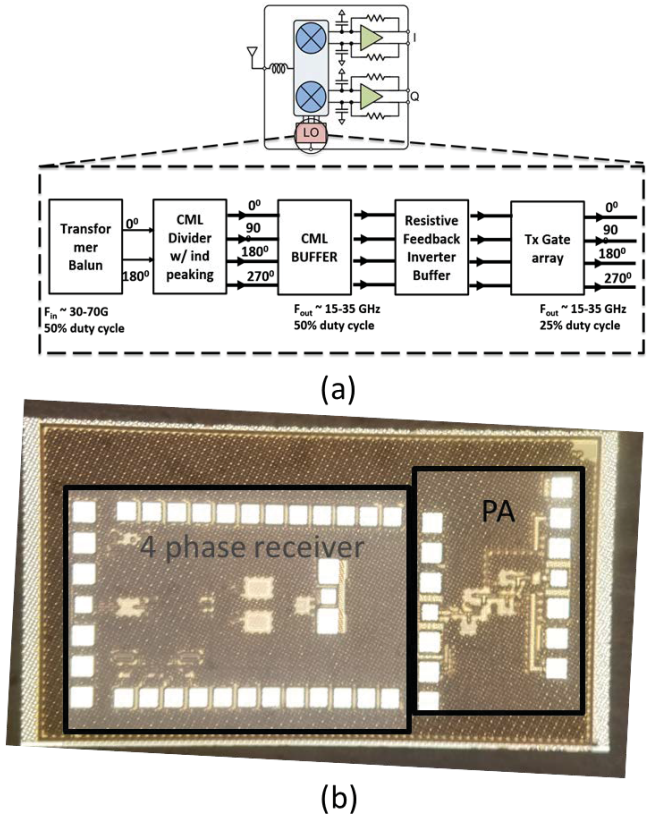


Figure 22: Gen-2 Four-Phase Receiver Block Diagram with LO Network Details (a) and Die Micrograph 1.6mm x 1.1 mm Receiver Area (b)

In addition to the revised LO network, we also slightly modified the mixer switches. From theory, if the switch resistance is slightly higher than the optimum value, the noise figure increases drastically. The degradation due to lower switch resistance is slower and smaller comparatively. Hence, in Gen-2 the switches were designed to have slightly smaller resistance (~19 ohms) and with parasitic resistances in layout the total on resistance is close to 20 Ω for a single switch. This resistance can be increased if required by changing the buffer supply or the input common mode. The drawback of this strategy is that the receiver hits worst case NF at a lower frequency than one sized with optimum width; however, it allows us to tune for the optimum resistance and achieve overall improved NF.

2.5.2 Gen-2 Measurement Results

The chip was received in July 2018 and was characterized using a measurement board with all DC and SPI pads wire bonded and RF pads wafer probed. This was done to improve the supply-plane network by introducing more pads. Also, the baseband amplitude and phase mismatch can be reduced and better controlled through printed circuit board (PCB)-based interconnects. Unlike Gen-1, the Gen-2 I and Q baseband outputs can be simultaneously measured as wire bonding removes the restriction coming from differential I and Q outputs. Figure 23 shows the evaluation board along with bonding diagram with symmetrical I and Q and multiple supply pads.

The chip was characterized through conversion gain, iP_{1dB}, and NF. Due to maintenance on our vector network analyzer (VNA), the input impedance is yet to be measured. Also, the conversion gain and linearity could be measured only up to 26.5 GHz. Our VNA was received back from repair in late August 2018 and will be used to complete the remaining measurements. Preliminary data is shared here.

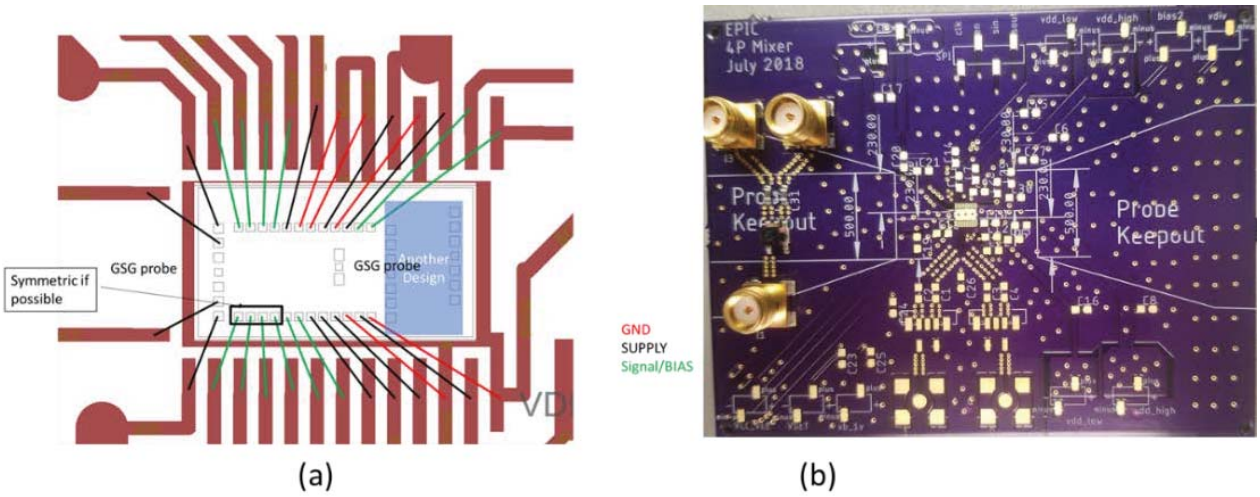


Figure 23: Bonding Diagram of the Gen-2 Chip (a) and Evaluation PCB for Gen-2 Chip-on-Board (b)

Power consumption of the Gen-2 receiver was 110 mW at 6 GHz LO and 220 mW at 30 GHz LO. Another 200 mW of power is consumed in the baseband output buffers used to drive 50 Ω loads. These are only present for test and would not be needed in a normal system.

Figure 24(a) shows the measured NF of the receiver from 6 GHz to 33 GHz. Above 33 GHz is not yet measured. Four different bias settings were used to cover the entire range in four frequency bands (6-10 GHz, 10-13 GHz, 13-26 GHz, and 25-33 GHz). Because of this, we observe discontinuities at the frequency boundaries. Figure 24(b) shows I channel noise is within 1 dB of Q channel noise, indicating that the error from Gen-1 is reduced. Note that NF does increase more rapidly with frequency than we expected from simulation. We are working to revise our simulation model to explain this behavior. Finally, we can compare Gen-2 to our very first 20-30 GHz mixer-first receiver which uses a passive LO generation scheme [Wil16]. Both exhibit a similar NF of 6-8 dB in the 20-30 GHz range.

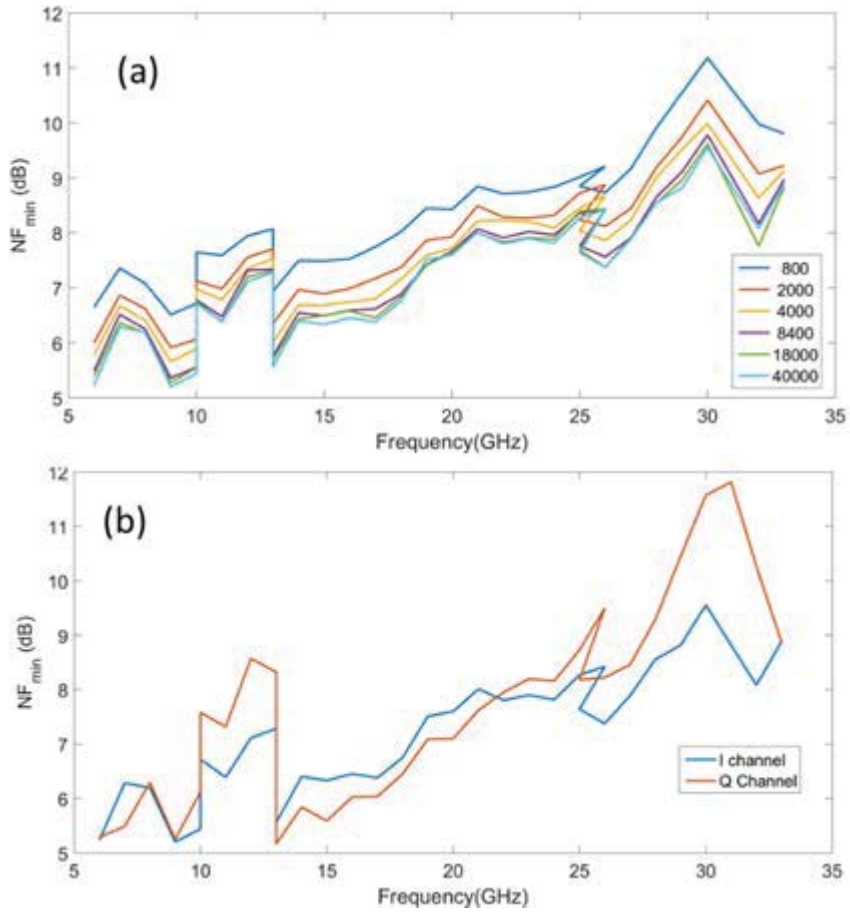


Figure 24: NF across Frequency for different Feedback Resistor Setting (b) I and Q NF for highest Feedback Resistor Setting and thus highest Gain Setting

As mentioned earlier, gain and linearity for Gen-2 were only measured up to 26.5 GHz. The results were measure with same bias settings that was used for NF measurements. Figure 25 compares the measured *output* P_{1dB} for Gen-2 and Gen-1. From this data, we see that the Gen-2 receiver has comparable linearity performance and operates to a much lower frequency as compared to Gen-1. Future measurements will allow us to confirm the maximum frequency, which we expect to be 35 GHz.

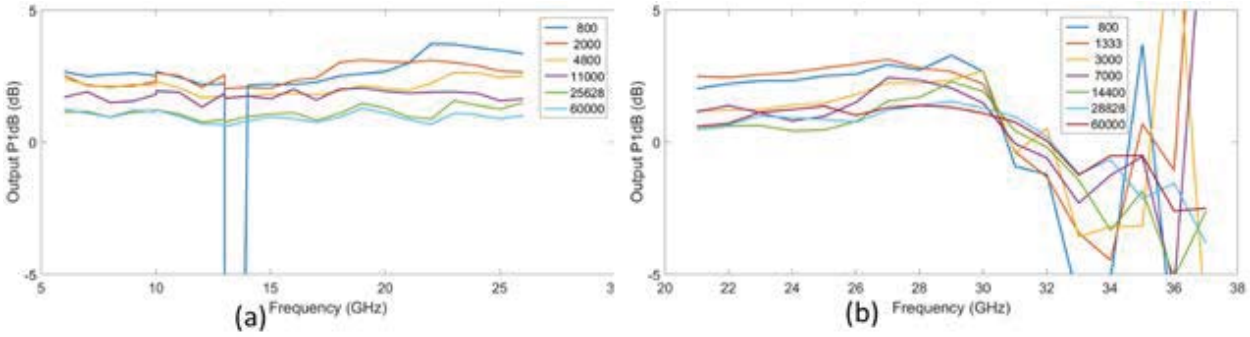


Figure 25: Measured Output P_{1dB} for Gen-2 Receiver (a) and Gen-1 Receiver (b) at 100 MHz Offset

Finally, Figure 26(a) shows the measured Gen-2 conversion gain as feedback resistance and LO frequency is swept. Gain is 21 dB, with I/Q gain error manifesting above 16 GHz. Figure 26(b) shows I and Q gain for 40k feedback resistance at 50MHz offset. The conversion gain plot shows the wide bandwidth of the receiver and very consistent broadband tuning capability. Note, however, that we observed that our bandwidth is not constant and reduces with increase in feedback resistance as shown in Figure 26(c)). This could be due to a negative capacitor which is introduced and controlled through amplifier frequency response. This is still under investigation.

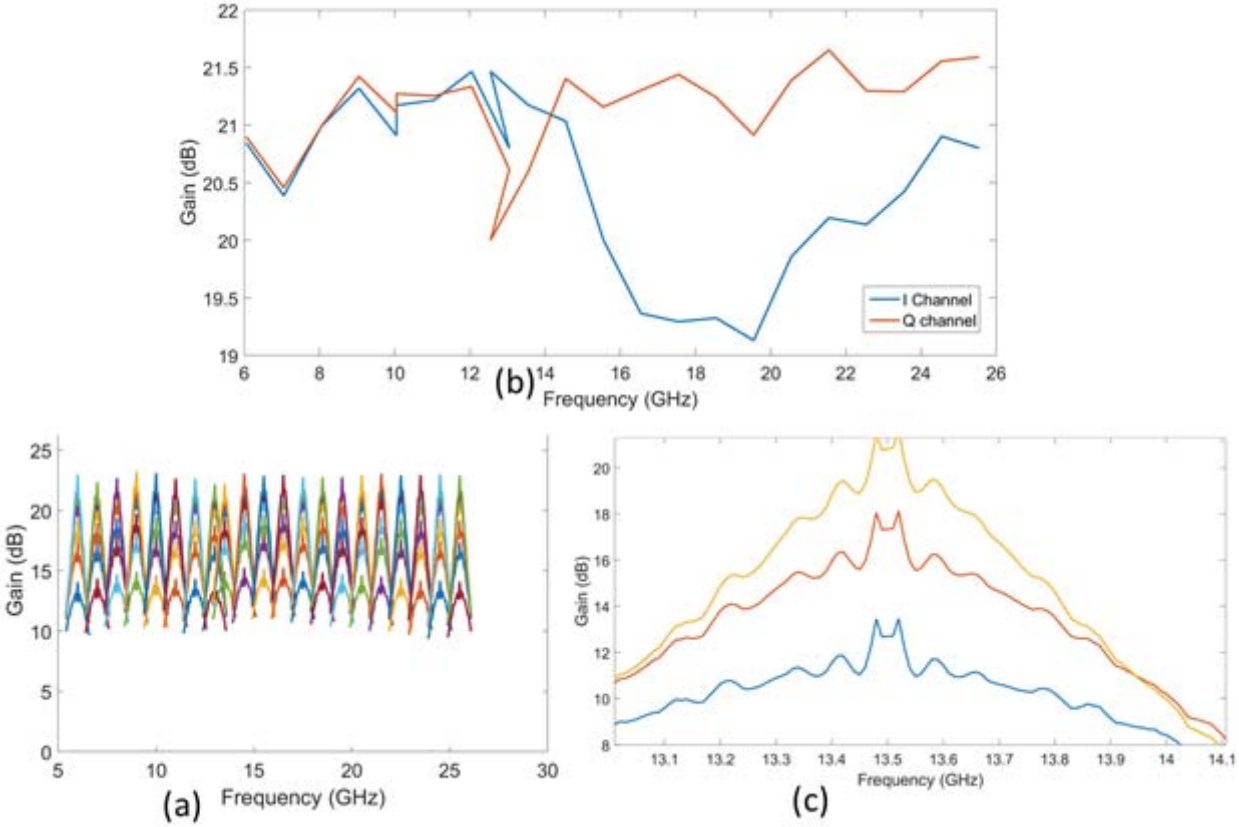


Figure 26: Conversion Gain vs. LO Frequency with RF swept from LO-600M to LO+600M for different Resistor Settings (a), I and Q Conversion Gain for 60K Resistance at 50 MHz Offset (b), and Zoomed-in Version of Conversion Gain Plot for three Feedback Resistances at 13.5 GHz (c)

2.6 Alternative Receiver Design

During this program, we had one Masters Student investigate an alternative receiver architecture. The purpose of this design is to explore whether reduced NF and wider bandwidths can be achieved when compared to a mixer-first topology. The schematic is shown in Figure 27. Note that this structure reverts back to a low-noise transconductor amplifier (LNTA)-first topology, where the LNTA is realized as a simple inverter-based cell. This preamplifier helps to reduce NF for the receiver and is inherently broadband. To provide input power matching, a translational negative feedback loop is created from the output of the baseband amplifiers to the RF input through a passive mixer with series resistor loads. Through simple tuning of the resistors, the

input impedance can be matched. Also, reactive tuning can be achieved through inclusion of coupling between quadrature phases. Stability of the loop is maintained by ensuring that loop gain is small (due to the resistive divider feedback ratio being small) and then forcing dominant pole compensation at the sampling capacitor of the mixer.

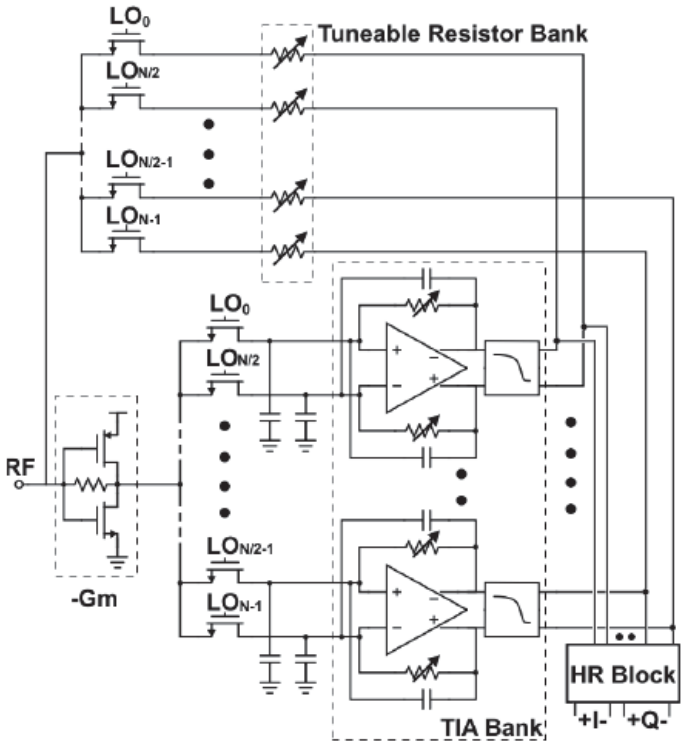
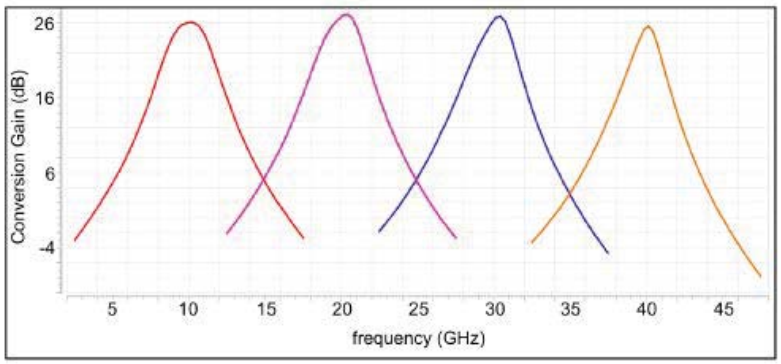
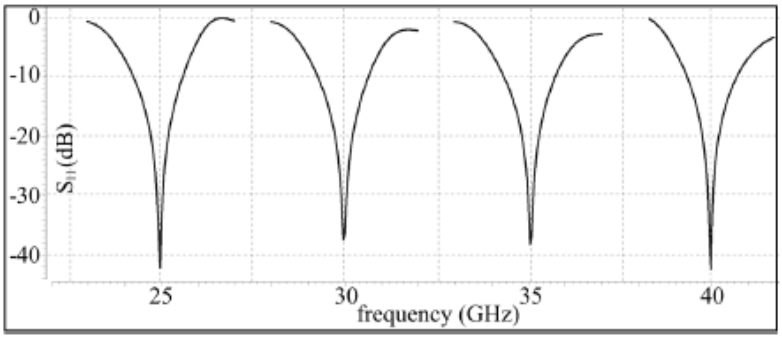


Figure 27: Block Diagram of Negative Feedback Wideband Receiver Employing LNTA and Passive Mixer Feedback

The simulated conversion gain and input matching (S_{11}) curves are shown in Figure 28(a) and 28(b). Here we use idealized LO networks. As can be seen, this receiver can provide gains of ~25 dB with input matching better than 10 dB. In Figure 29(a), we compare the simulated NF of the feedback receiver to that of a simple mixer-first receiver (using ideal LO signals, meaning no LO buffers). Here, we see that the feedback receiver can improve NF by over 1 dB (due to inclusion of the LNTA cell). In Figure 29(b), we show simulated NF versus LO frequency. NF still increases beyond 30 GHz due to LNTA limitations. Simulated input P_{1dB} is -15 dBm whereas iIP3 is -5 dBm.



(a)



(b)

Figure 28: Simulated Conversion Gain and S_{11} of Alternative Receiver as LO Frequency is swept and using idealized LO Network

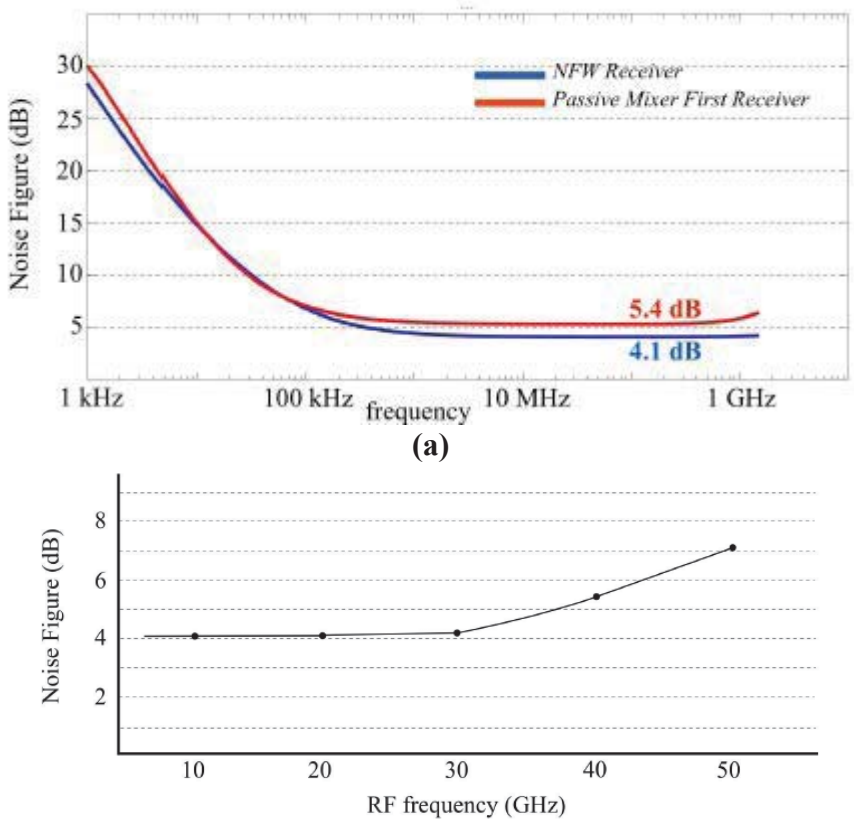


Figure 29: Simulated comparison between Mixer-First Receiver (red) and Negative Feedback Receiver (blue) (a) and simulated NF vs. LO Frequency for Negative Feedback Receiver (b)

This circuit architecture shows promising performance and will be investigated as part of the future DARPA program, Millimeter-Wave Digital Arrays (MIDAS).

2.7 Summary of EPIC CORE Receiver Results

Table 1 presented earlier summarized the total measurements for our three generations of mixer-first receivers. Key conclusions drawn from our receiver research are as follows:

- Broadband receiver operation of 6 to >33 GHz is ultimately achieved in Gen-2, consistent with our modified program goal. This receiver can exhibit consistent gain with increasing NF across the band (ranging from 5 to 9 dB). Frequency selectivity is set by the LO frequency and the baseband bandwidth.
- The design of the LO network is the key limiter for achieving broadband operation. We took three iterations to get this LO network properly designed and optimized.
- Four-phase mixer-first receiver outperforms eight-phase mixer-first receivers for 10-16 GHz. As such, a four-phase design appears suitable for X, K, and Ka band operation.
- The broadband LNA can achieve 5 dB NF, 20 dB gain, and -16 dBm iP_{1dB} for 24-44 GHz. The four-phase mixer-first receiver can achieve 6-8 dB NF, 10-20 dB gain, and -12 to -3 dBm iP_{1dB} for 5-33 GHz. A cascaded LNA plus four-phase mixer would therefore have

5.1 dB NF, 30-40 dB gain, and -32 to -23 dBm iP_{1dB}. As a result, we conclude that the four-phase mixer-first receiver has superior dynamic range; thus, the LNA appears unnecessary for the EPIC platform.

- In simulation a LNTA-first receiver with passive mixer feedback exhibits reduced noise figure and potentially higher operating frequency. This architecture will be studied in future programs.

3. THRUST 1B: CORE TRANSMITTER RESEARCH AND DEMONSTRATION

The goal of this sub-thrust is to design and realize a multi-purpose transmitter IP CORE which has the flexibility to work with any beamformer at any frequency. This core can serve as a direct upconversion stage for beamformers which operate at the same frequency as the core (i.e., from 10-32 GHz). Alternatively, the core can serve as a first upconversion stage in a superheterodyne architecture, in which the beamformer includes a second upconversion to final frequencies above 32 GHz.

Discussion is organized according to the two generations of receivers which were implemented. A first design and tape-out (Gen-1) was completed in April 2017 with measurements completed by January 2018. A second design and tape-out (Gen-2) was completed in May 2018 with hardware still being manufactured.

A summary of the final results is provided here in Table 3. These results will then be discussed in detail in the following section. In summary, our first-generation transmitter core did not function properly and the error was traced to a problem in the custom design of our coupler components used for baluns and quadrature generation in the LO network. The transmitter was redesigned and achieves most program goals, falling short on the minimum frequency range (though we will still measure down to 10 GHz). Notably, the Gen-2 transmitter exhibits high output power and wide bandwidth.

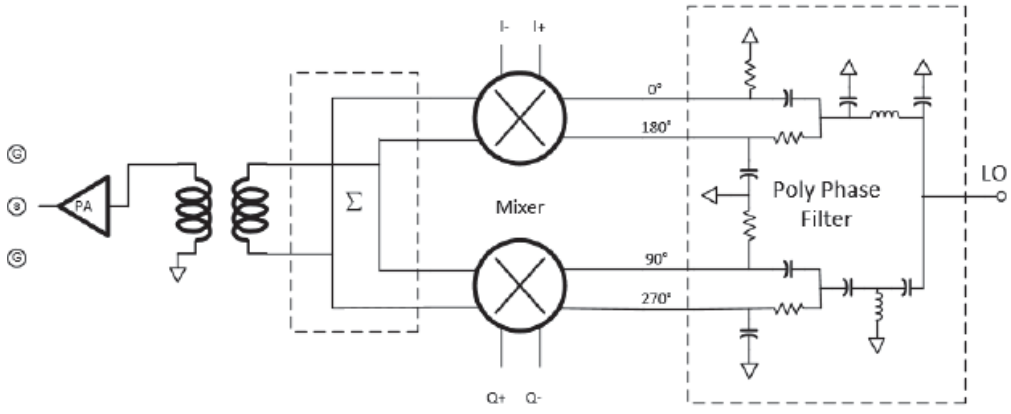
Table 3. Comparison of Key Transmitter Results to Modified EPIC Target

	Gen-1 (Sim)	Gen-1 (Meas)	Gen-2 (Sim)	EPIC Target
Freq. Range	26-34 GHz	27-29 GHz	20-33 GHz	15-32 GHz
Conversion Gain	16 dB	-45 dB	19.5-24.4 dB	20-35 dB
oP_{1dB}	>+12 dBm	NA	16.7-19.3 dBm	+12 dBm
Image/LO Suppression	20/40 dBc	10/-- dBc	30/36 dBc	20/40 dBc

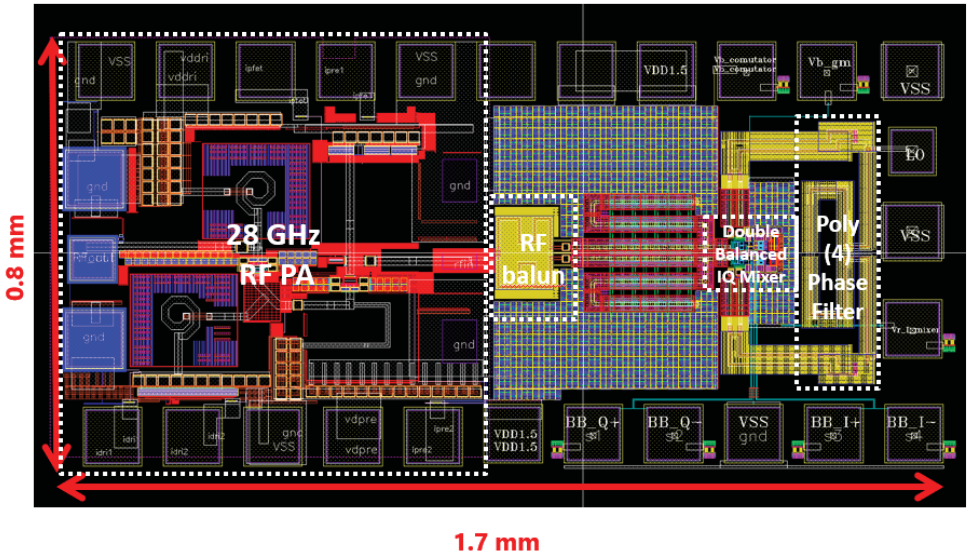
3.1 Gen-1 Transmitter Design

Gen-1 transmitters were taped out in April 2017 and most measurements were completed by January 2018. The transmitter for the Gen-1 CORE does not have a prior Gen-0 measurement result on which to base our design. As a result, we worked to mitigate risk, adopting the following strategy. First, since we already had designed and measured a 28 GHz PA with acceptable output power (~17 dBm) prior to the start of the DARPA program, this PA was used within the transmitter with slight modification to attempt to broaden the bandwidth and broaden the S_{22} response. Second, we based our mixer designs on a set of prior upconversion mixers from a 30 GHz intermediate stage of a 94 GHz transmitter. Finally, in Gen-1 we did not attempt to achieve a full 10-32 GHz operation and focused instead on narrow-band range around 28 GHz.

A block diagram of the overall transmit chain is shown in Figure 30(a) and a layout screenshot in Figure 30(b). The baseband I and Q phase inputs are provided through off-chip BB buffers (not shown). Active Gilbert-cell quadrature mixers upconvert the signal to the 24-30 GHz range. The RF output is then connected to a single unbalanced PAs through an on-chip balun. Note that in the layout, we included GSG pads at the interface between the mixer and the PA to allow for in-situ characterization of both. The quadrature LO signals for the mixer are derived from a custom passive polyphase network based on a couple transmission lines designed using EM simulations. In Gen-2, this LO network will be replaced with the active LO generation.



(a)



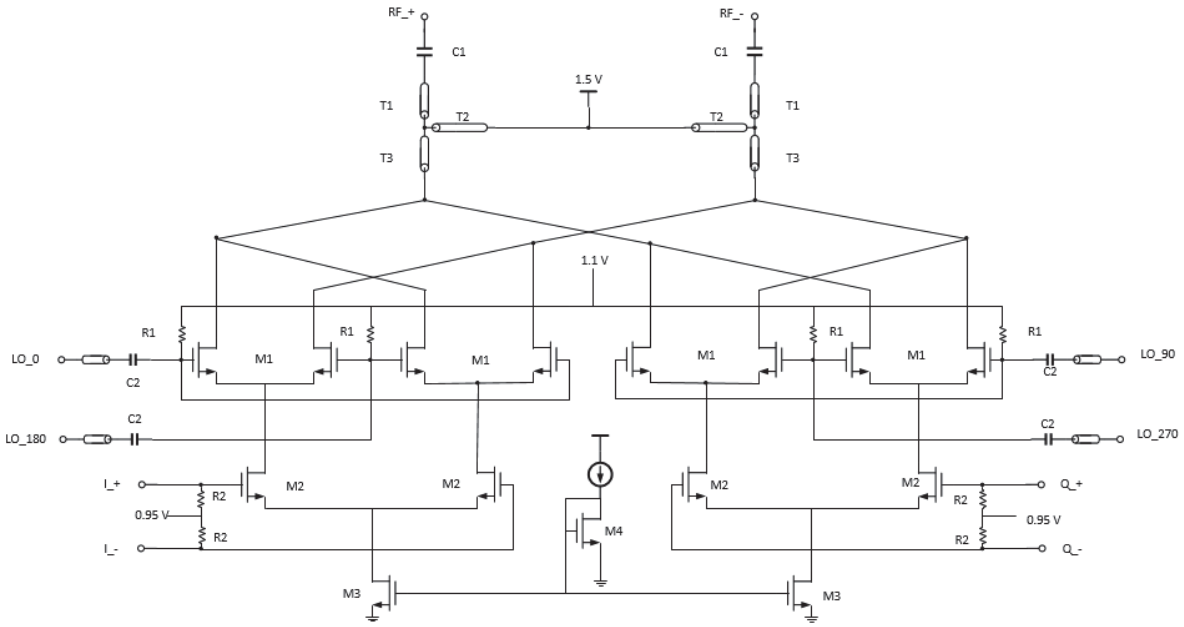
(b)

Figure 30: Block Diagram of the Transmitter for the CORE (a) and Layout Screenshot of Transmitter (b)

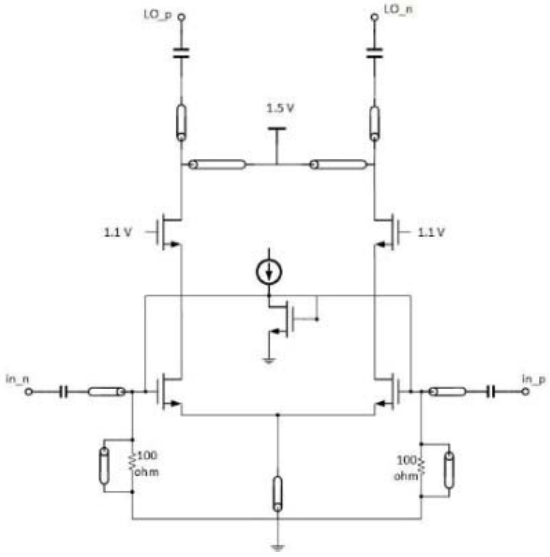
Note that the PA can be characterized individually as can the upconversion mixer.

A schematic for the upconversion mixers is shown in Figure 31(a). The modulator is composed of two current-combined Gilbert-cell based double-balanced mixers. Differential outputs are combined using a transformer to create a single-ended output. Simulations for the mixer indicated a conversion gain of approximately 10-13 dB across 25-29 GHz with output P_{1dB} greater than +5.5 dBm.

The LO signals are fed to the mixer using the active buffer shown in Figure 31(b). This buffer uses a differential cascode topology with transmission-line based resonant loads. Simulations show that the LO buffer achieves roughly 10 dB gain centered at 29 GHz, with 3 dB bandwidth greater than 10 GHz.



(a)



(b)

Figure 31: Schematics of Gen-1 Single-Sideband Upconversion Mixers (a) and LO Buffer (b)

The quadrature input signals for the LO signals are generated using a passive polyphaser filter. This filter is composed of a coupled-line balun to generate differential signals and then two quadrature generators again composed of coupled-line structures. These were custom designed using EM simulation. As will be discussed later, an error in the metal stack-up file used by the

designer of this filter resulted in greatly overestimated coupling between layers. As a result, the filter was incorrectly designed and will not work for the intended frequency range.

A schematic of the two-stage power amplifier is shown in Figure 32. In both stages, a cascode structure having thin-oxide common source and thick-oxide common gate is used. This allows larger voltage swing at the output and supports higher output power. A combination of both transmission line and inductor-based matching is used, selected to minimize area. According to simulation, the PA achieves 20 dB gain, peak power added efficiency (PAE) of 36%, output 1dB compression of +17 dBm, and saturated output power of +18 dBm.

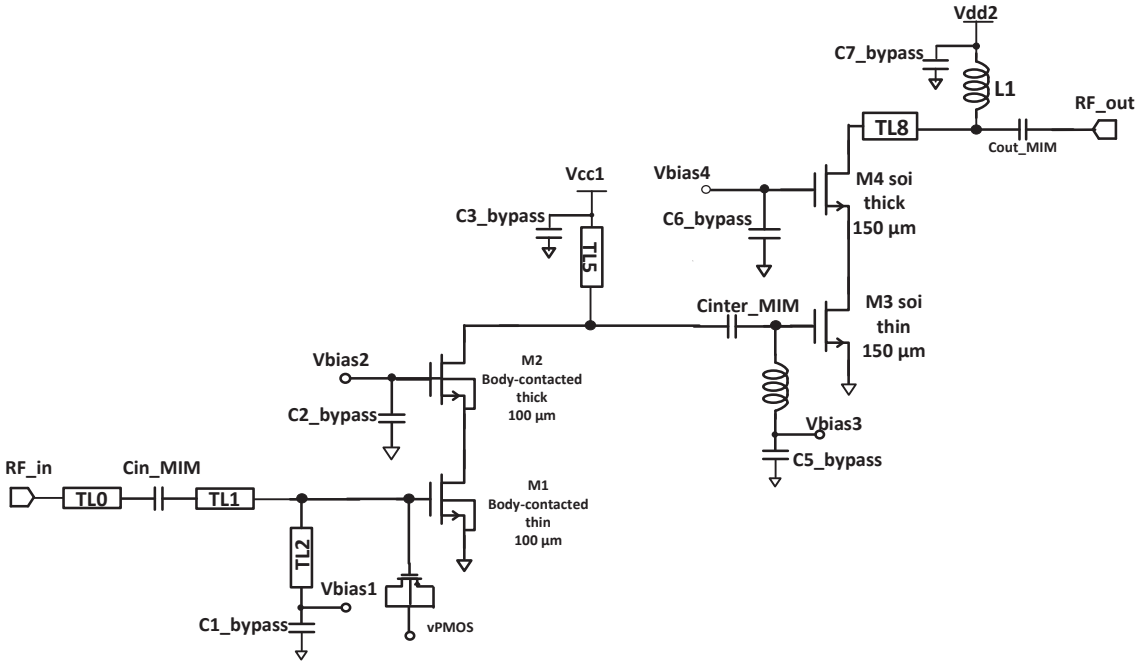


Figure 32: Schematic of Gen-1 Power Amplifier

The full simulated results for the Gen-1 transmitter are summarized in Figure 33. In simulation, the TX provides 16 dB total conversion gain, 19.7 dB image suppression and greater than 40 dB LO feedthrough suppression. Improved image suppression can be achieved through baseband signal optimization.

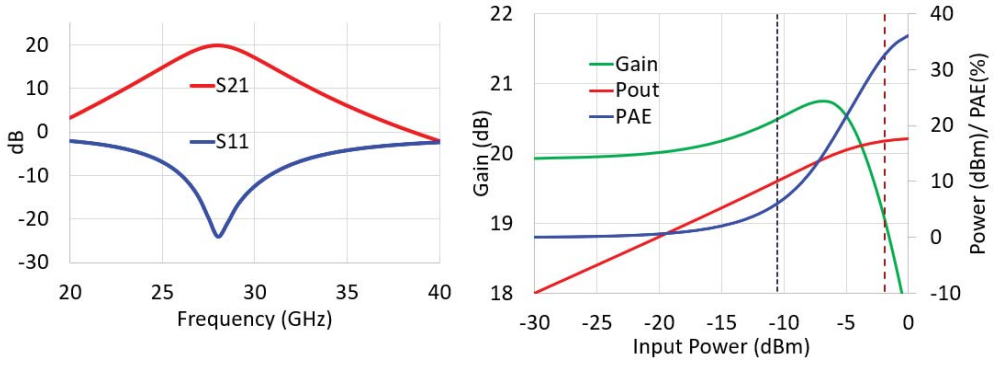
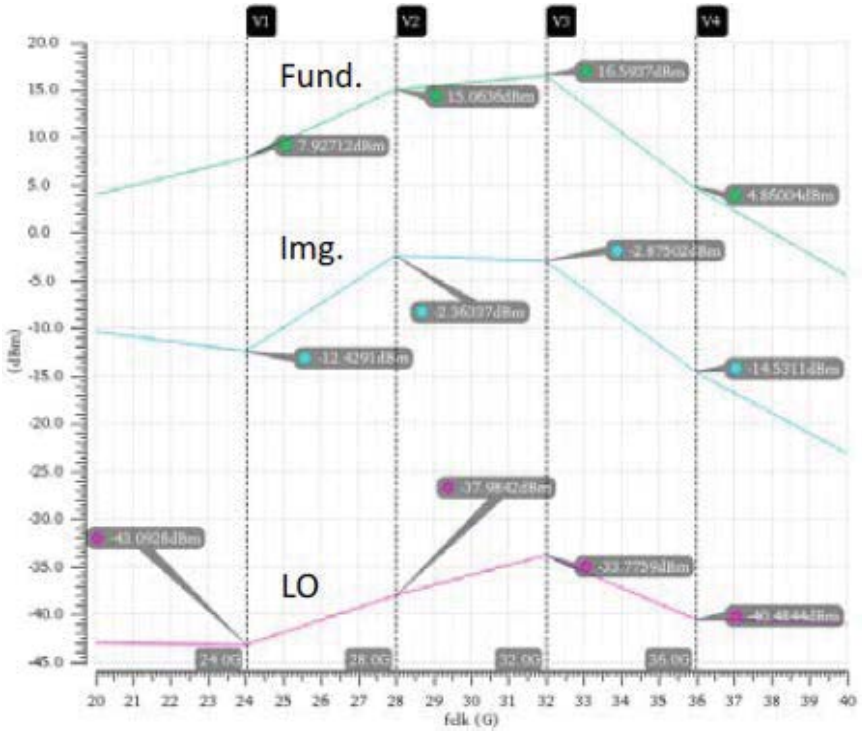
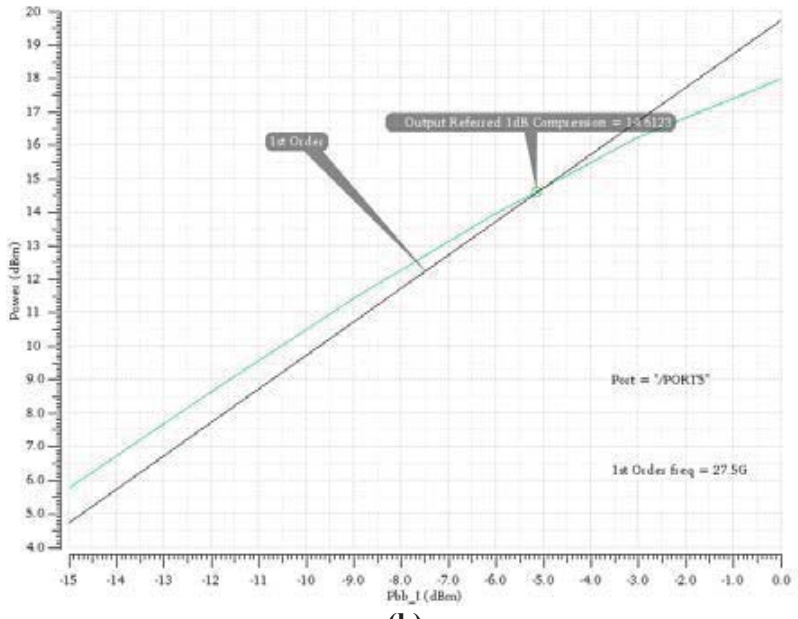


Figure 33: Simulated S-parameters and Swept-Power Plot (gain, PAE, Pout) for the Gen-1 PA

A plot of the output power, LO feedthrough, and image power across frequency is shown in Figure 34(a). In terms of frequency response, the transmitter can provide greater than +12 dBm output power across a 26 to 34 GHz frequency range. The output P1dB at 28 GHz is +14.6 dBm, as shown in Figure 34(b). This is less than the compression point of the PA alone, where the limit is coming from the output power of the mixer.



(a)



(b)

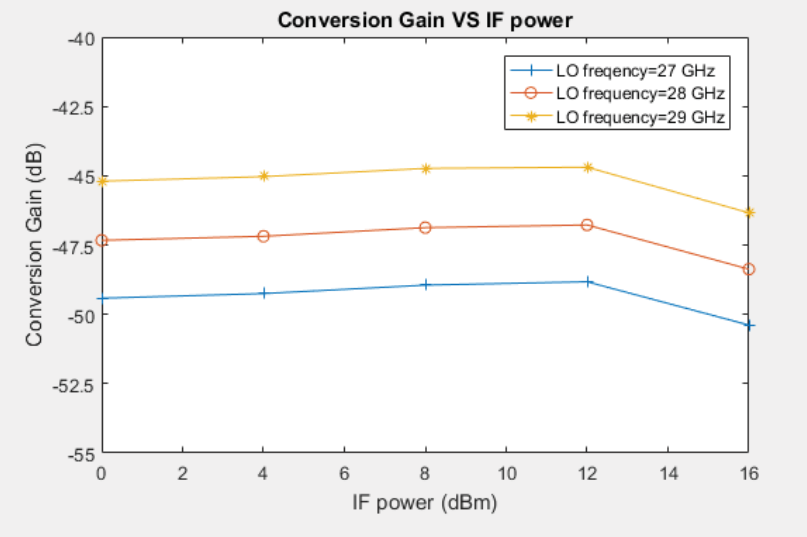
Figure 34: Simulated Output Power, Image Power, and LO Feedthrough Power when IF is driven with -1 dBm Signal at 500 MHz (a) and Simulated Swept Power Plot of Transmitter indicating +14.6 dBm oP$_{1dB}$ (b)

3.2 Gen-1 Transmitter Measurements

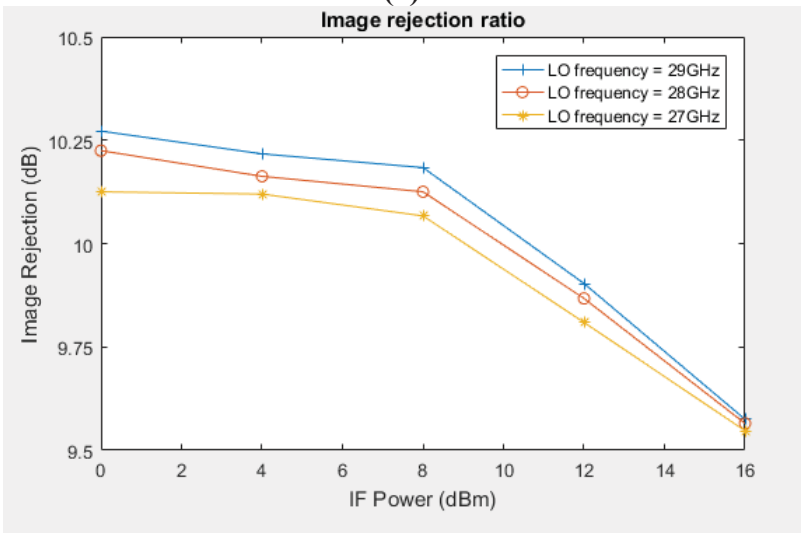
3.2.1 Results

The Gen-1 transmitter measurements were completed by January 2018. A custom PCB was created to allow wirebonding of DC signals and probing of RF signals. Our Gen-1 transmitter did not work properly. The mixer and the PA were first measured together and then separately. From a DC standpoint, we found that all the DC biasing conditions for the mixer and the PA first stage are very close to simulation; however, the PA second stage has biasing inconsistently compared to the simulation condition. We traced this biasing error to the current mirror for the second stage.

Our measurement results indicate that the baseband signal is upconverted, however the output RF signal power is at a very low level. These measurement results for conversion gain and image rejection are shown in Figure 35. Conversion gain is extremely low at -45 dB. Image rejection is around 10 dB. By adjusting different biasing conditions and trying chips on multiple boards we confirmed that the mixer is upconverting but there are problems which lead to a very low power levels as well as mismatched differential RF signals.



(a)



(b)

Figure 35: Measured Gen-1 Mixer Conversion Gain (a) and Image Rejection (b)
LO input power is +10 dBm at 27, 28, and 29 GHz.

3.2.2 Gen-1 Transmitter Debugging

We discovered a design flaw within the mixer, specifically within the custom-designed passive components used to create the quadrature for the LO and to provide a balanced-to-unbalanced conversion at the mixer output. These structures were realized using transmission-line based couplers, designed using Momentum. We discovered that the layer stack-up used by the designer for these parts had an error. In particular, the distance between the topmost layers, LB and UB, was incorrect, caused by a "growing" of the layers toward each other, leading to a much closer spacing and much stronger coupling. As a result, both the LO quadrature network and the mixer output balun have considerable loss and phase error in the target band.

We then used the correct stack-up definition file, but now simulated what was taped out in Gen-1. The amplitude response of the LO quadrature generation network is shown in Figure 36(a). The phase shifts (not shown) are no longer in differential quadrature and loss is 18-23 dB. The balun used between the mixer and PA has the same problems, showing 10 to 20 dB loss at 30 GHz, as shown in Figure 36(b). These errors cannot be fixed or overcome for the Gen-1 hardware; thus, we had to focus efforts on a Gen-2 revision.

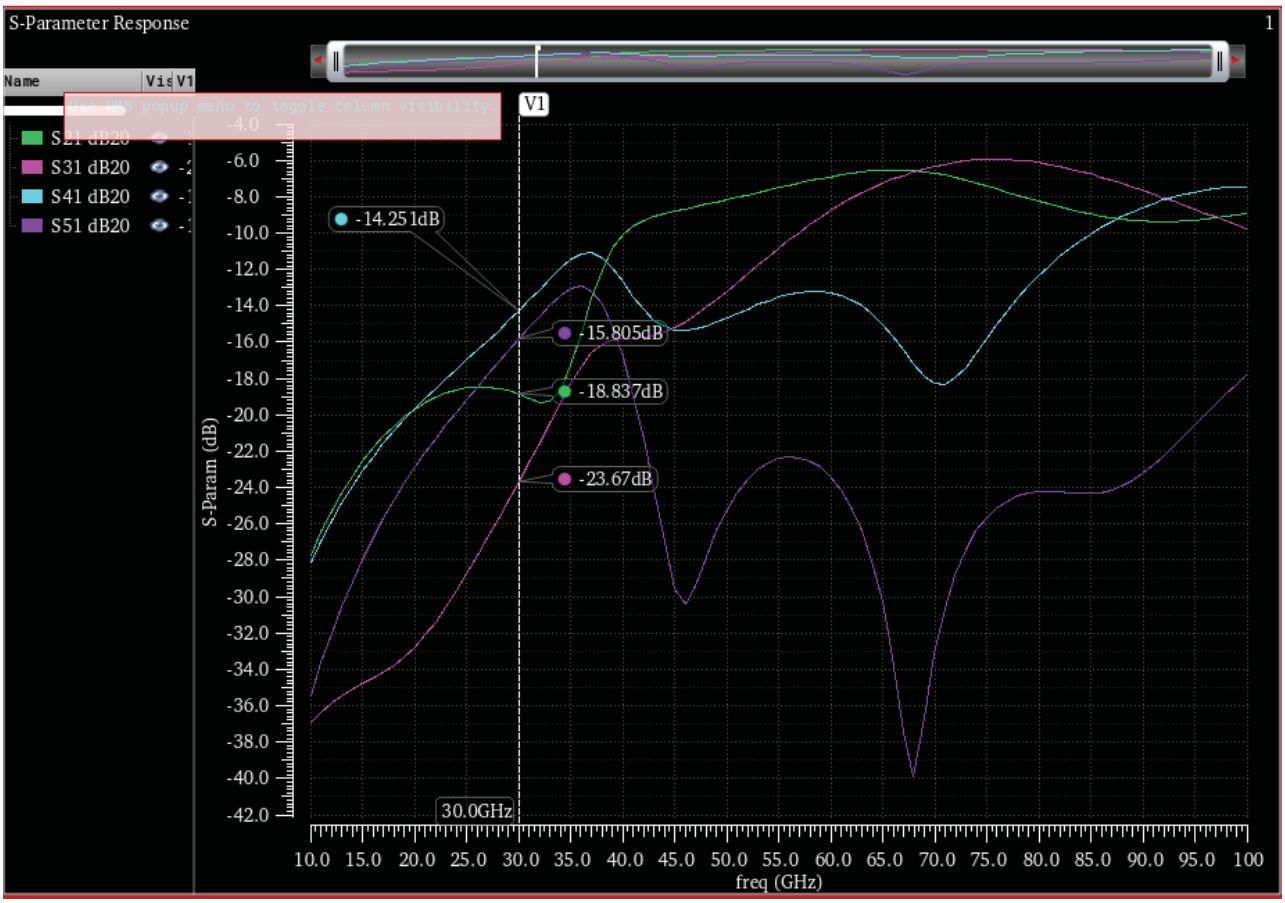


Figure 36(a)

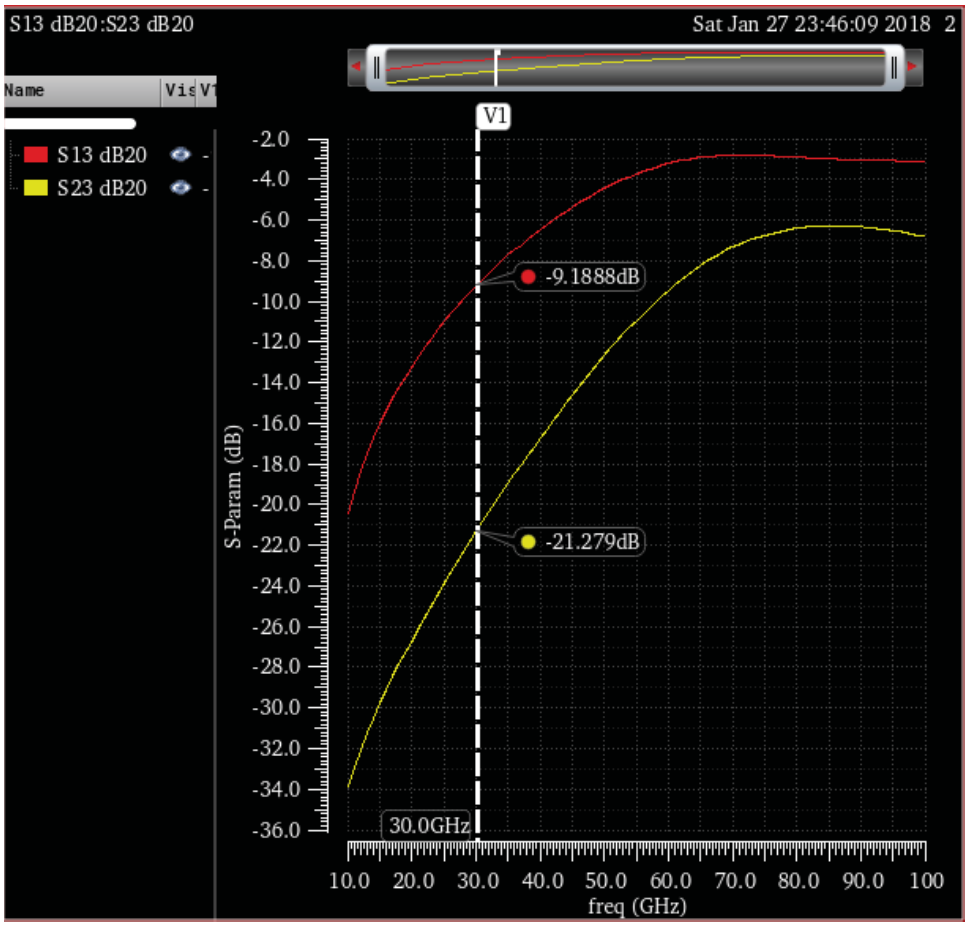


Figure 36(b)

Figure 36: Simulated Amplitude Response of the LO Quadrature Network (a) and the Balun used between Mixer and PA (b)

These simulations are completed using the correct stack-up, showing incorrect optimization.

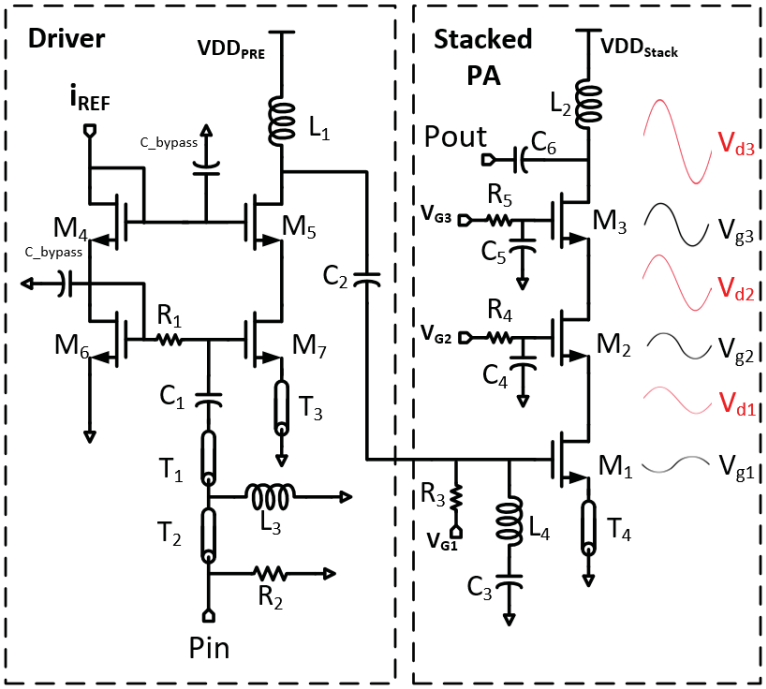
3.3 Gen-2 Transmitter Design

3.3.1 Power Amplifier Design and Tape-out

The Gen-2 transmitter design was split between two tape-outs in GF 45RFSOI. We included a break-out of the Gen-2 PA on a first tape-out on February 2018, which was the same date as the Gen-1 receiver tape-out. Due to time and resource limitations, the full transmitter was not ready for this tape-out; thus, it had to be shifted to the next available tape-out which occurred on May 2018.

The Gen-2 PA was completely redesigned to target 20-33 GHz bandwidth with >18 dBm oP_{1dB} (differential 100 Ω) across the band. A schematic of the Gen-2 PA is shown in Figure 37. The first/predriver stage of the PA uses a simple cascode with 1.5 V supply voltage and providing ~8 dB power gain. The output stage uses a triple-stacked topology to achieve 15 dBm output power per each PA half. Stacking enables a higher composite breakdown voltage and thus supports higher output power with a load impedance equal to 50 Ω per half. This impedance avoids the need for any output matching and thus allows broadband operation using a simple

inductive RF choke. We investigated two-, three-, and four-stack architectures and found the three-stack to have best performance. Thick-oxide gate FETs are used in the second and third devices within the stack to allow an increased supply voltage of 3.6 V. Finally, as with other device stacking, bootstrapping is used to allow the gate voltage of M2 and M3 to follow the input voltage and avoid local breakdown-voltage conditions. This bootstrapping is provided using capacitors to ground on each gate which together with the C_{gs} of the transistor provide a capacitive voltage divider. Large-valued resistors isolate the gate from the DC bias connection.



(a)

(b)

Figure 37: Schematic (a) and Layout Screenshot (b) of the Gen-2 PA

In simulation the PA achieves 31% peak PAE and over 20 dB gain. The output P_{1dB}, saturated output power, and PAE are shown versus frequency in Figure 38(a) for a single-sided output of the PA. The differential output power would be 3 dB higher. Across 20-33 GHz, the oP_{1dB} (differential) is 16.7-19.3 dBm. PAE hits a maximum value of 32% around 27 GHz. Saturated output power (differential) is 19-21 dBm.

Figure 38(b) shows small-signal s-parameters, again confirming broadband operation. The bandwidth can be measured using the frequency range over which saturated output power is within 1 dB of peak, corresponding to 44% bandwidth (23 GHz to 36 GHz). Alternatively, the small-signal 3 dB bandwidth is 40.7% (20.4 GHz to 32.7 GHz) as shown in Figure 38(b).

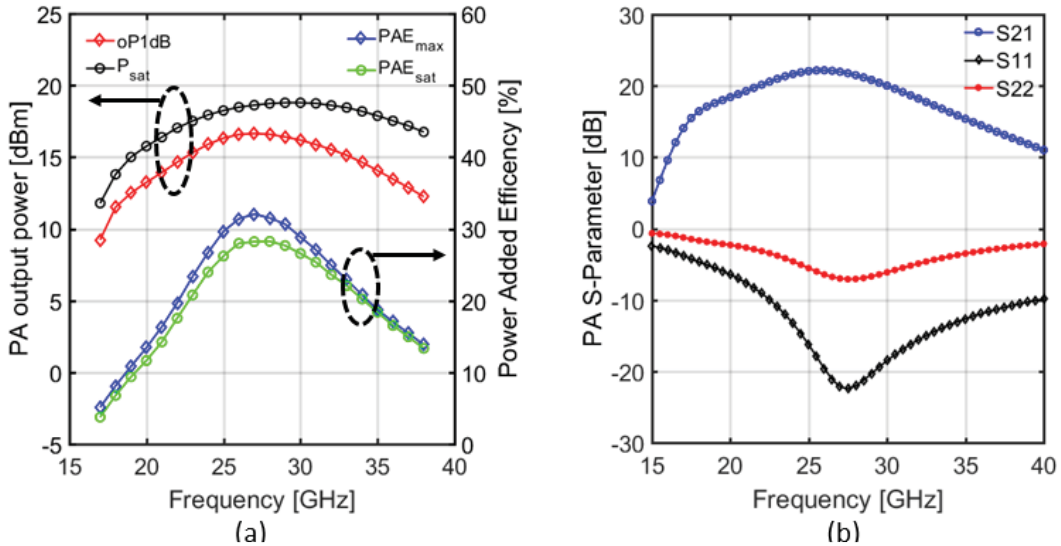


Figure 38: Simulated oP_{1dB}, Psat, and PAE vs. Frequency (a) and Simulated S-parameters of Gen-2 PA (b)

3.3.2 Full Transmitter Design and Tape-out

As mentioned, the Gen-2 transmitter design was split between two tape-outs in GF 45RFSOI. The full transmitter was taped out on May 2018 and is still in fabrication.

A block diagram of the Gen-2 transmitter is shown in Figure 39. The active LO generation from the Gen-2 receiver is used to provide broadband quadrature LO signals and to be compatible with the receiver if integrated together into a single transceiver. A revised single-sideband mixer stage is used followed by the Gen-2 balanced PA described above. Fully differential signaling is used throughout, avoiding the need for any baluns and saving area. The PA output is kept differential for flexibility.

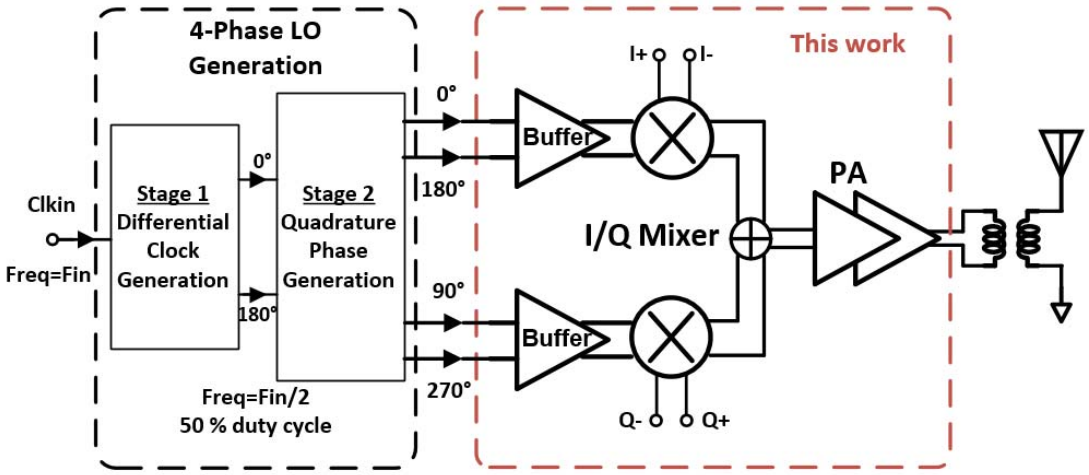


Figure 39: Gen-2 Transmitter Block Diagram

3.3.3 Gen-2 Transmitter LO Network

Figure 40 shows a simplified diagram of LO network, which is slightly revised compared to the network used in the Gen-2 receiver. A single off-chip LO provides reference clock at twice the LO frequency to an on-chip balun. Differential clocks are then divided by two to generate quadrature-phase outputs. Two tuned cascode-based LO amplifiers are placed close to the mixer switch gates to provide sufficient swing from 500 mVpp to 1.5 Vpp while reducing common-mode amplitude mismatch. A broadband tuned load is used at the buffer output. To achieve target bandwidth, R1 and R2 are used to decrease the quality factor value of matching which decides the achievable bandwidth at the cost of lower gain and more power consumption.

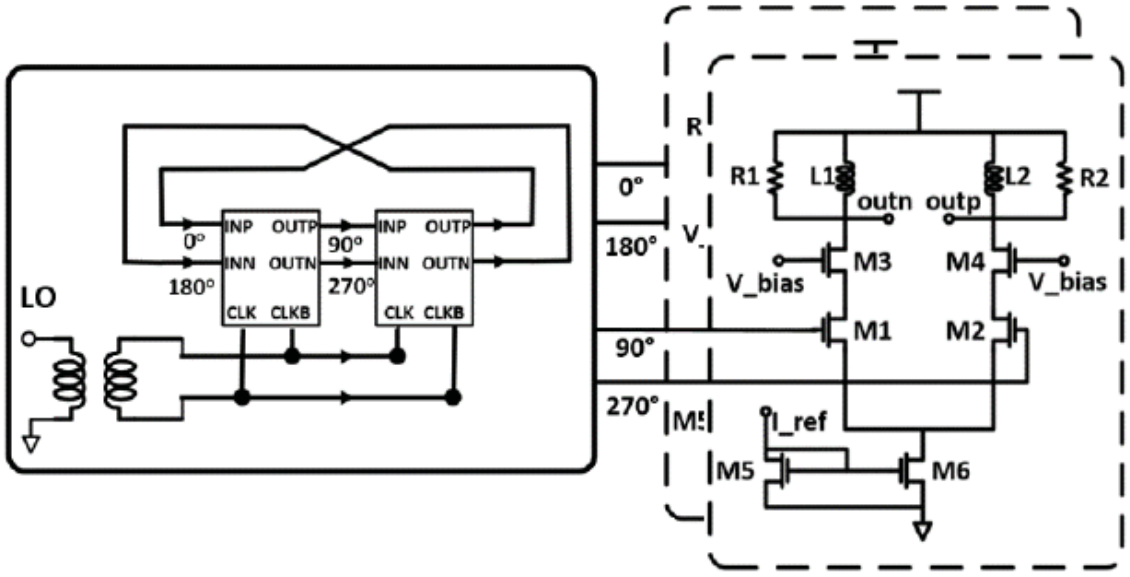


Figure 40: Schematic of Gen-2 LO Network for Transmitter

The simulated results of this LO network are shown in Figure 41. From this, we see that the output amplitude is above 0.5 V from 18 to 34 GHz. With a +5 dBm reference LO, the output differential LO power adjusted from 3 dBm to 12 dBm by varying I_{ref} from 1mA to 4mA. As shown in Figure 41(b), the IQ phase error is simulated to be less than 2.5 degree and calculated image rejection ratio (IRR) is more than 32dB within entire band.

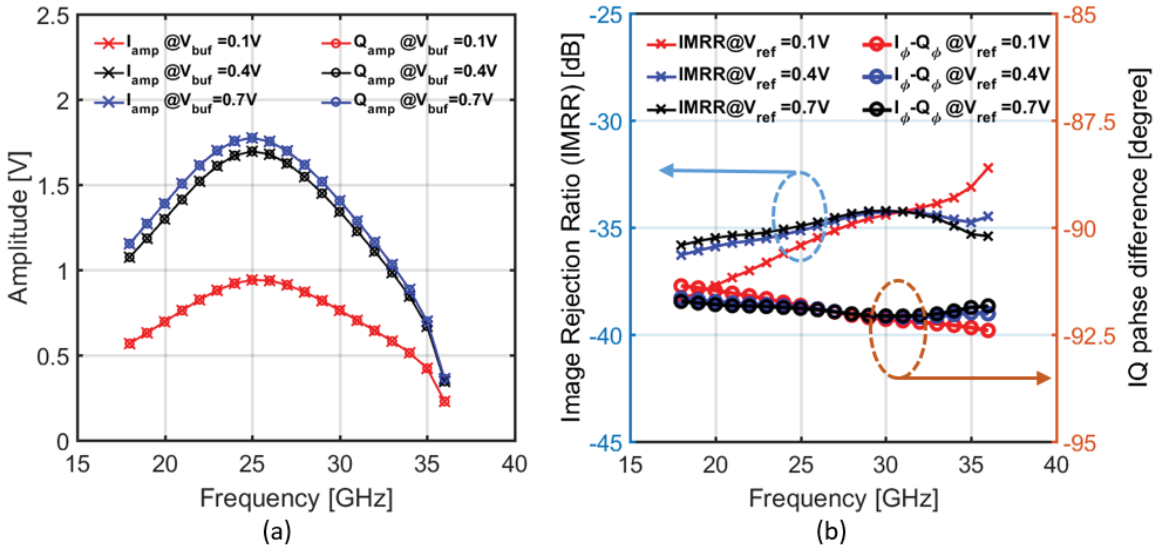


Figure 41: Simulation Results of Quadrature Clock Generation for Gen-2 Transmitter

3.3.4 Gen-2 Single-Sideband Mixer

Figure 42 shows a schematic of the Gen-2 mixer. As in Gen-1, it is based on a double-balanced Gilbert cell which provides good port isolation and image rejection. The mixer transconductor stage is resistively degenerated to improve input power handling capability and increase modulation signal bandwidth. Transducer NMOS (M5, M6) are sized 60µm/40nm to achieve moderate conversion gain over target band. Commutator (M1 to M4) are sized 21.15µm/40nm for fast switching and low feed through.

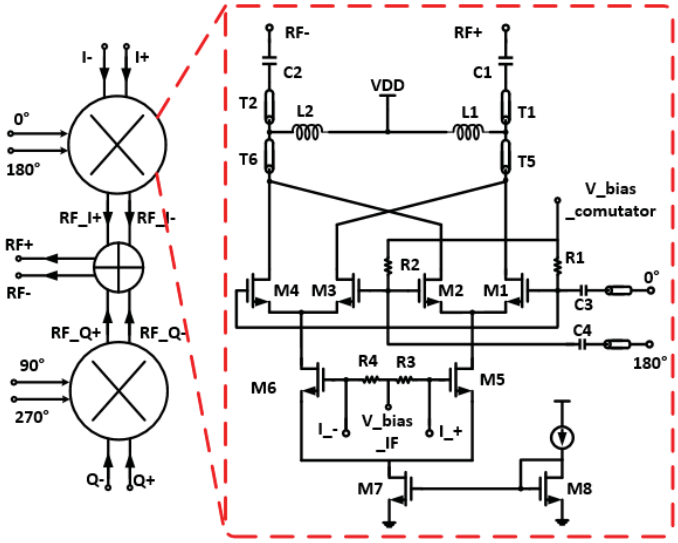


Figure 42: Schematic of Gen-2 Mixer

In simulation, the mixer draws 28 mA current from a 1.6 V supply. Simulation results in Figure 43 show the mixer conversion gain can be adjusted from 0 to 4.6 dB over 18 to 35 GHz. LO and image suppression are more than 31 dB and 33 dB respectively.

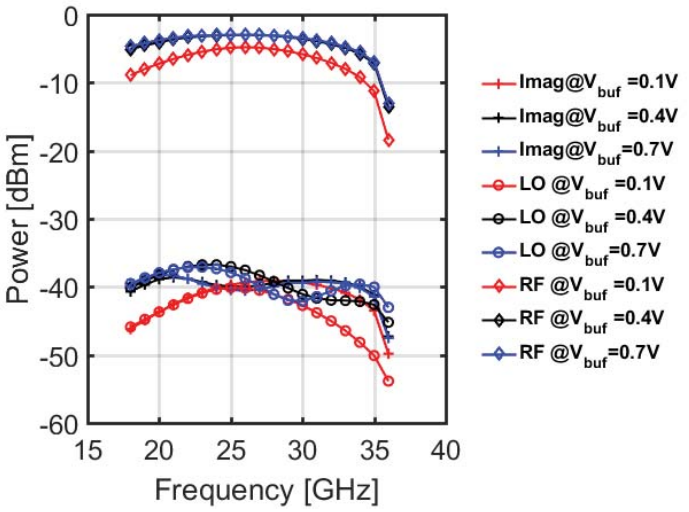


Figure 43: Simulated RF Output Power, LO Leakage and Image Sideband of Gen-2 Mixer

3.3.5 Gen-2 Transmitter Simulations

A layout screenshot of the Gen-2 transmitter is shown in Figure 44. From left the right, we have the PA, mixer, and LO network. Total chip area is 1.6 mm x 1.9mm including the pads (0.7 mm x 1.3 mm active area only).

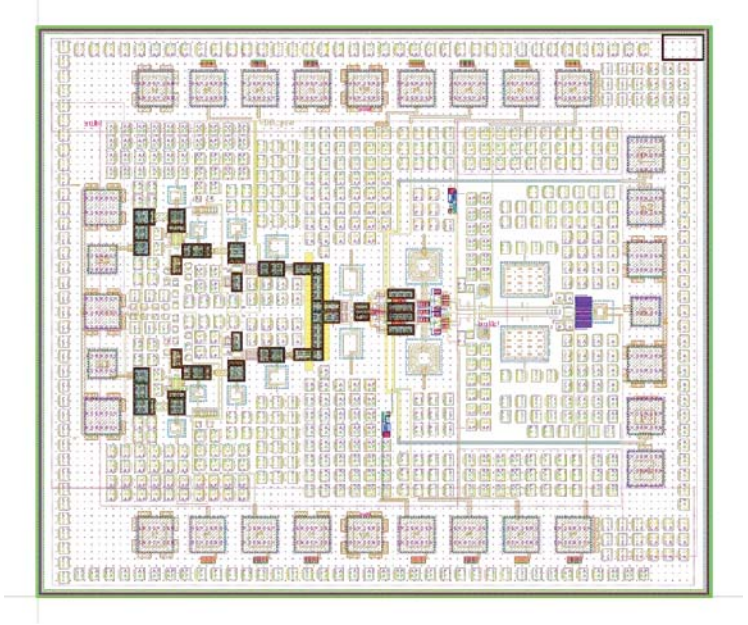


Figure 44: Layout Screenshot of Gen-2 Transmitter

End-to-end simulations were completed for the Gen-2 transmitter. The results for RF, image and LO feedthrough at transmitter output are shown in Figure 45(a). Differential conversion gain is 19.5-24.4 dB and oP_{1dB} ranges from 16.7 to 19.3 dBm over 20-33 GHz. Modulation bandwidth is more than 3.5 GHz before it is limited by the bandwidth of the signal trace from pad to mixer input. The RF bandwidth is mainly limited by the PA stage. Image rejection and carrier suppression are more than 30 dB and 36 dB at the transmitter output. All results are reported for the differential output of the transmitter, and for a single ended output, the power will be 3 dB lower as shown in earlier.

A transient simulation with a baseband IQ source is performed to further characterize the transmitter. Figure 45(b) shows the simulated error vector magnitude (EVM) for the transmitter for 16-QAM modulation at 1Gb/s. Calculated EVM is around 9.4% with output RF power at 4.5 dB back off from oP_{1dB} (13.5 dBm).

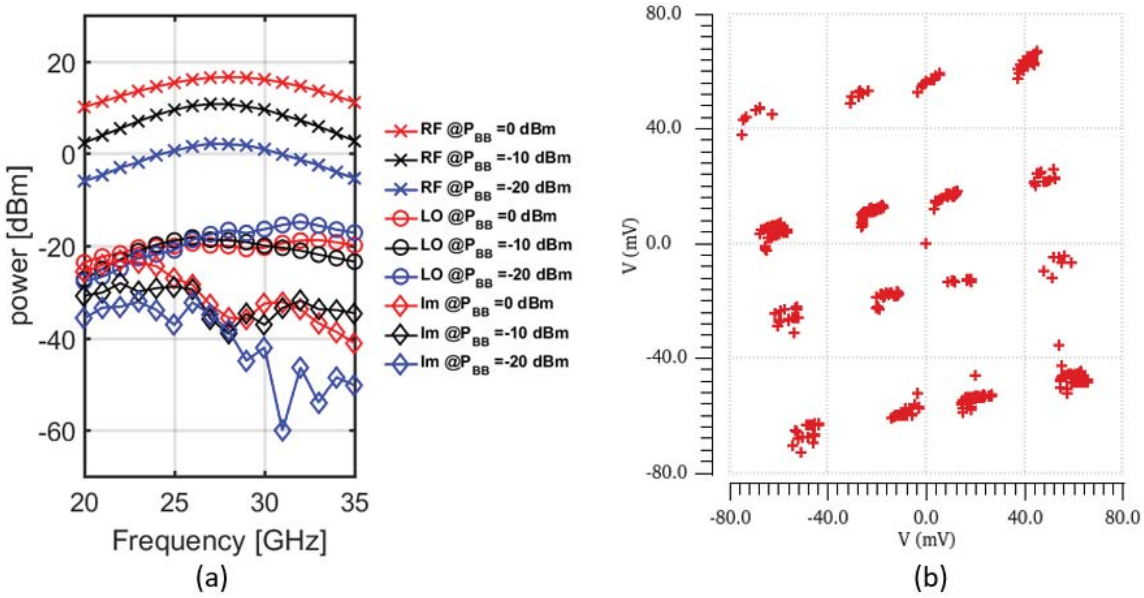


Figure 45: Simulated Results for Gen-2 Transmitter

Output power, LO leakage and image band vs. swept LO frequency for input baseband powers of -20/-10/0 dBm (a) and constellation for 1Gb/s 16-QAM data (b).

3.4 Gen-2 Transmitter Measurements

We received our Gen-2 PA breakout from the February 2018 tape-out in summer 2018. It has not yet been measured due to two factors. First, our Gen-2 receiver was being characterized. Second, the VNA broke and was out for repair for six weeks. We have just received (September 2018) the repaired VNA and are now proceeding to measurement of the Gen-2 PA. The Gen-2 transmitter has not yet been received and is still being fabricated.

4. THRUST 2: MILLIMETER-WAVE BEAMFORMING EXTENDERS

The goal of this thrust is to design and evaluate beamforming extenders operating at 28, 60, and >80 GHz. The 28 and 60 GHz EXTENDERS are realized under industry-funded parallel project. The >80 GHz EXTENDER is realized within EPIC.

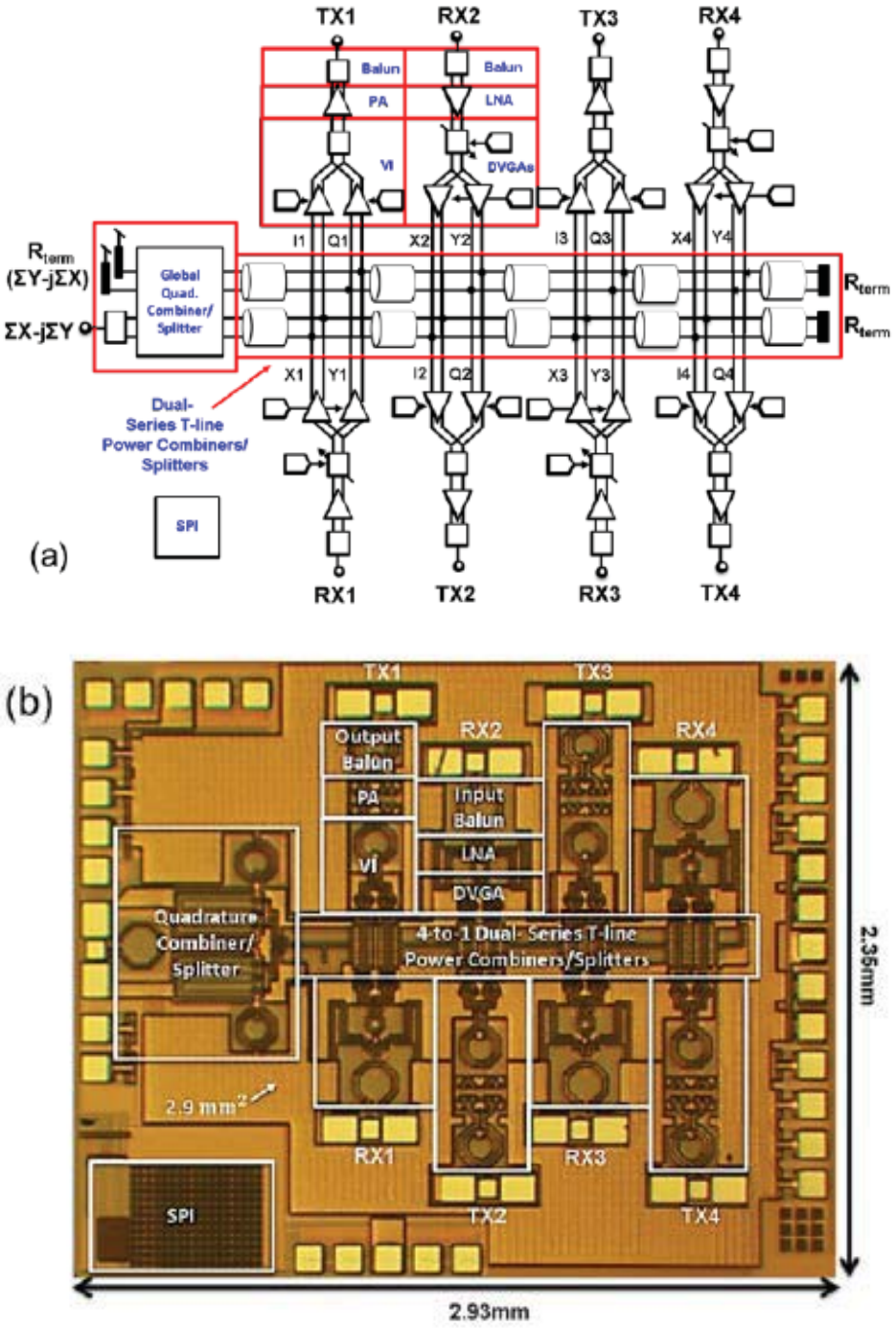
Thrust 2 is subdivided into three sub-thrusts, as follows:

- Thrust 2A focuses on a 28 GHz transceiver array developed with funding from Analog Devices. Use of this EXTENDER will allow the CORE to be tested in direct-conversion receive/transmit modes.
- Thrust 2B focuses on >80 GHz transmit array with frequency conversion from 30 GHz to >80 GHz. Use of this EXTENDER will allow the CORE to be tested in superheterodyne transmit mode.
- Thrust 2C focuses on a 60 GHz receive beamformer developed with funding from Samsung. Use of this EXTENDER will allow the CORE to be tested in a subharmonic receive mode.

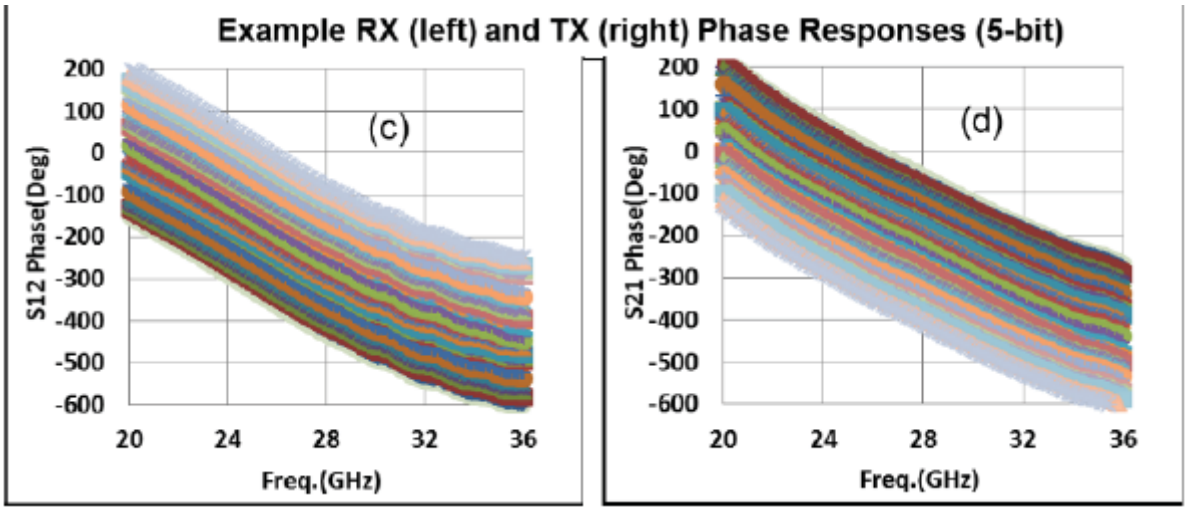
Below, we briefly report the measured results for thrusts 2A and 2C and include detailed information on thrust 2B, in which we designed and measured 150 GHz beamformer components in SiGe 9HP and designed an 80 GHz signal chain in SiGe 8HP which is still being manufactured.

4.1 Thrust 2A (28 GHz EXTENDER)

We completed wafer-level characterization of our 28-GHz "dual-vector distributed beamformer" which was implemented in GF SiGe BiCMOS 8HP technology. Figure 46(a) and 46(b) show a block diagram and photo of the beamformer. A four-element transceiver array is integrated together with a series-feed network. Each front end includes RF amplifiers, and a pair of variable-gain amplifiers (VGAs). A global quadrature combiner is used for global interpolation and beamforming, allowing for reduced area and potentially broader bandwidth. The measured phase responses are shown in Figure 46(c) and 46(d) for five-bit control for receive and transmit modes. Good performance is seen across the frequency range. We did observe an issue in this beamformer in the transmit chain, where the VGAs' resonant frequency is not aligned with the PA resonant frequency. This was fixed in a new version of the circuit. A summary of measured performance results is shown in Figure 46(e). Further details can be found in [Yeh17] for the original circuit.



(Figure 46 continued on next page)



(e)

Technology		130-nm SiGe
Phase Shift Type		Dual-vector
Frequency (GHz)		24-28
Phase Resolution		5-bit
TRX Phase Error (°)		< 4.2
TRX Gain Error (dB)		< 0.5
RX Gain (dB)		8.7 to 11.5
RX NF (dB)		4.5 to 6.9
RX iP_{1dB} (dBm)		-25.4 to -18.4
RX iIP_3 (dBm)		-15.1 to -9.1
TX Gain (dB)		9.4 to 14.3
TX oP_{1dB} (dBm)		4.2 to 9.6
TX P_{sat} (dBm)		12.1 to 16.4
DC Power (mW)	(RX)	121.5*
	(TX)	165*
Area (mm^2)		0.2**(RX) 0.15**(TX)

Figure 46: Block Diagram of Second-Generation 28 GHz Beamformer (a), Die Photograph (b), Measured 5-bit Phase Response in Receive Mode (c), Measured 5-bit Phase Response in Transmit Mode (d), and Performance Summary Table (e)

4.2 Thrust 2B (>80 GHz EXTENDER)

Thrust 2B underwent modifications over the course of the program. Initially, our plan was to focus on a 94 GHz EXTENDER to leverage prior PA work. At program kickoff, this target was changed to 150 GHz based on mutual interest. As a result, the Gen-1 beamformer for Thrust 2B targeted 150 GHz and was designed in GF SiGe 9HP technology. This hardware was taped out in October 2016 with measurements completed in August 2017. As we will show, there were significant disagreement between model and hardware above ~120 GHz in 9HP. Upon seeing these results, we realized that obtaining good performance at 150 GHz would take two more tape-outs, which would place this activity over budget and off schedule. As a result, we decided to move the Gen-2 transmit beamformer to 80 GHz in SiGe 8HP. This allowed us to leverage existing circuit blocks from Floyd's research group which had been fully characterized as part of

a 76-81 GHz radar transceiver [Fuj17]. These components were then used to create a single-channel transmit chain with 30 GHz input, upconversion mixer, and 80 GHz power amplifier output. This still will allow us to evaluate the EPIC transmitter platform with frequency conversion within the EXTENDER. Arguably, the actual frequency is of secondary importance. The Gen-2 EXTENDER was taped out in May 2018 in GF SiGe 8HP and is still being fabricated.

4.2.1 Gen-1 150 GHz Transmit EXTENDER Design

Figure 47 shows a block diagram of the targeted Gen-1 single-element 150 GHz EXTENDER. A 30 GHz IF signal is upconverted to 150 GHz through mixing with a 120 GHz LO signal. This LO signal is derived from an X4 multiplier comprising two cascaded frequency doublers. Buffers are used to provide a strong LO signal to the mixer. Finally, a four-stage PA is used at the output, targeting +14.5 dBm saturated output power at 150 GHz. In the Gen-1 tape-out, three individual blocks were realized, each designed for wafer probing. These blocks are marked with boxes in Figure 47 - the 60-to-120 GHz doubler with LO buffer, the 30-to-150 GHz upconversion mixer, and the four-stage PA chain. Simulation results for each are reported below.

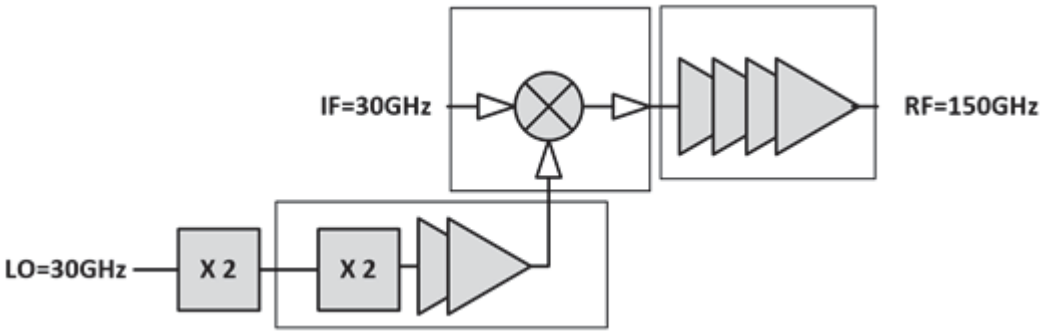
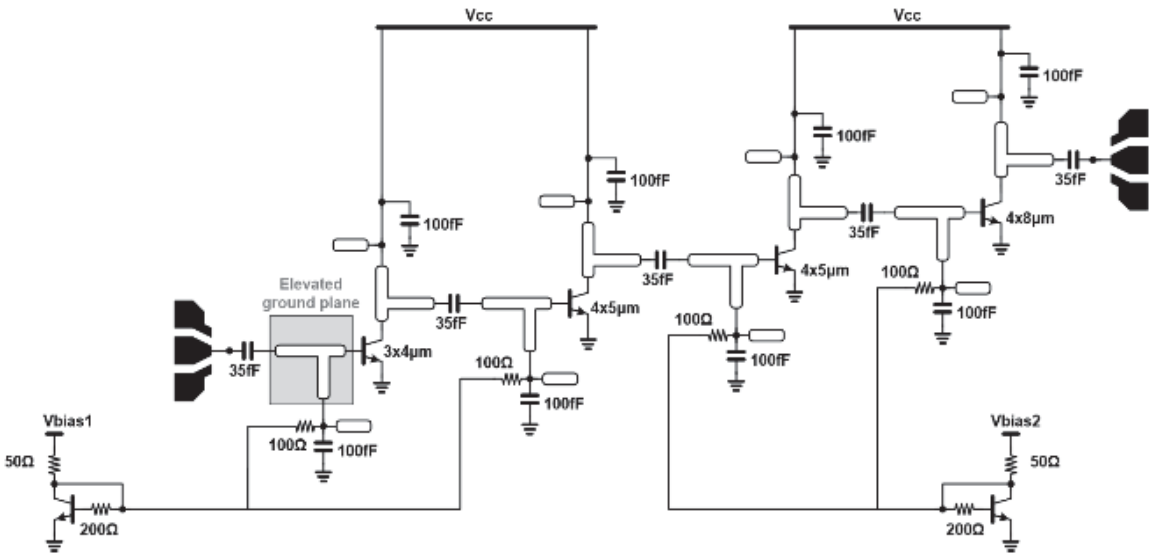


Figure 47: Block Diagram of 150 GHz Single-Element EXTENDER

Prior to designing any individual circuit, we first completed measurements on test structures realized in a previous SiGe 9HP run. These structures included transmission lines and metal-insulator-metal capacitors. Measured results were compared with EM simulations to validate our methodology for this technology. Good agreement was seen between hardware and simulation.

4.2.1.1 PA Breakout

The PA is a four-stage design, with schematic and die photo shown in Figure 48. Transmission-line matching networks are used together with MIM capacitors for each stage. All passive elements of the design are EM simulated both in ADS Momentum and ANSYS HFSS. The final simulated performance is summarized in Figure 49. Saturated output power is 14.5 dBm (28 mW), peak PAE is 7.8%, and DC power is 352 mW. The s-parameters indicate broadband gain and input/output matching responses.



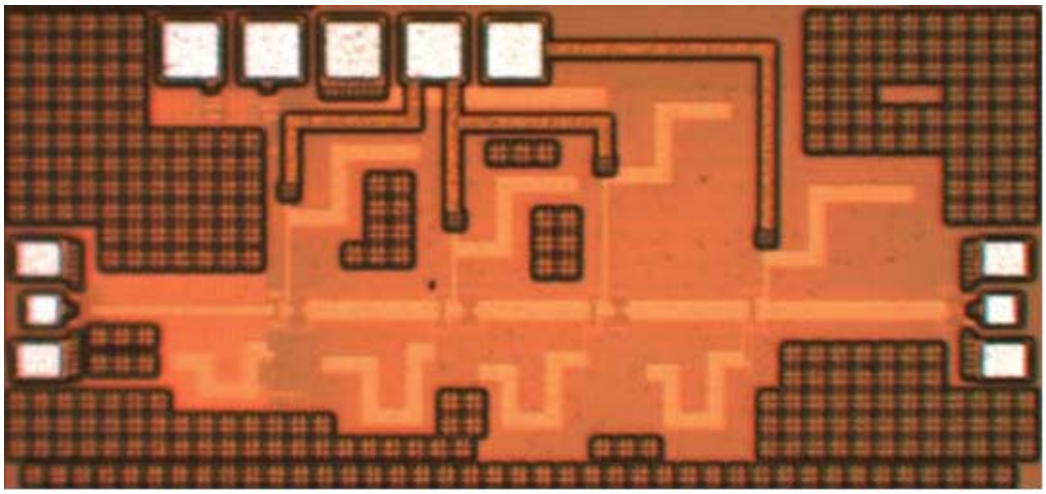
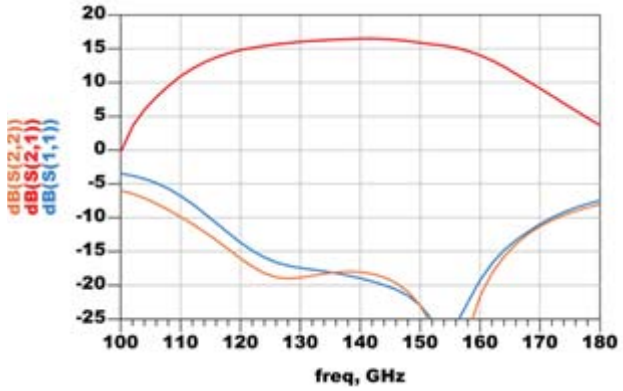


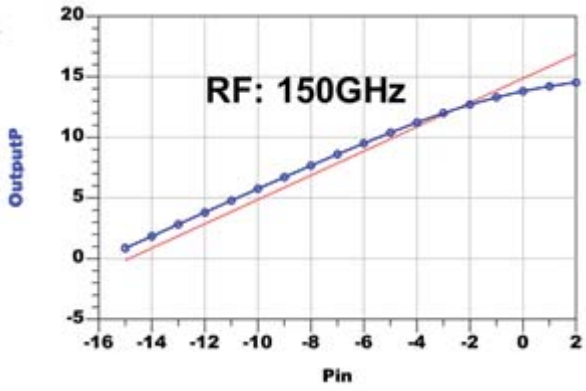
Figure 48: Schematic Diagram (top) and Chip Photograph (bottom) of the 4-Stage PA

Performance Summary	
# Stages	4
3dB BW	120GHz – 160GHz
Psat	14.5dBm ≈ 28mW
SS gain	15dB
Pdc	352mW
Efficiency	7.8% (PAE)
Area	1275µmx600µm

(a)



(b)



(c)

Figure 49: Performance Summary Table for 150 GHz PA (a), Simulated S-parameters (b), and Swept Power (c)

4.2.1.2 Mixer Breakout

The mixer is an active commutating structure, with schematic and photo shown in Figure 50. The design is based on a standard Gilbert mixer topology with t-line impedance matching on all three ports and on chip Marchand baluns on the RF and LO ports to convert differential on-chip signals to single-ended external equipment. All EM structures are custom designed. A performance summary table is shown in Figure 51. The output power versus frequency is shown for -20 dBm input power in Figure 51(b), indicating a peak conversion gain of 8 dB. The swept PIPO plot is shown in Figure 51(c) for final extracted simulation, indication output P_{1dB} of -12 dBm.

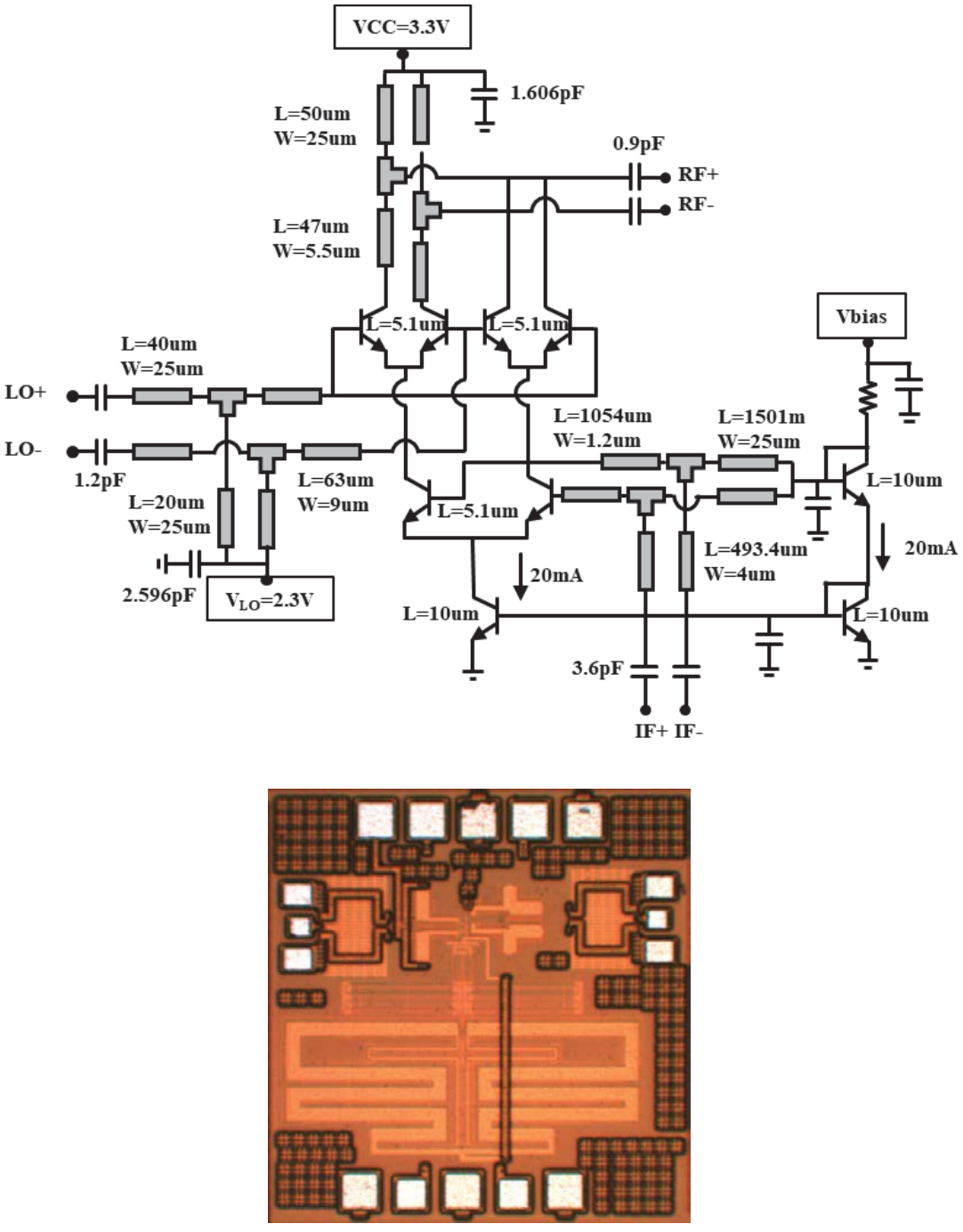
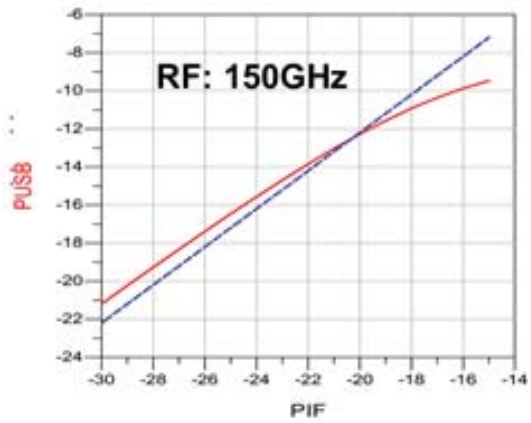


Figure 50: Schematic Diagram (top) and Chip Photograph (bottom) of the Up-Converting Mixer

Performance Summary	
Conversion Gain	8dB
IF Bandwidth	25GHz – 35GHz
LO Bandwidth	120GHz – 130GHz
LO power	1dBm
P1dB (Output)	-12dBm
Image rejection	10dB
Area	700µmx350µm

(a)

(b)

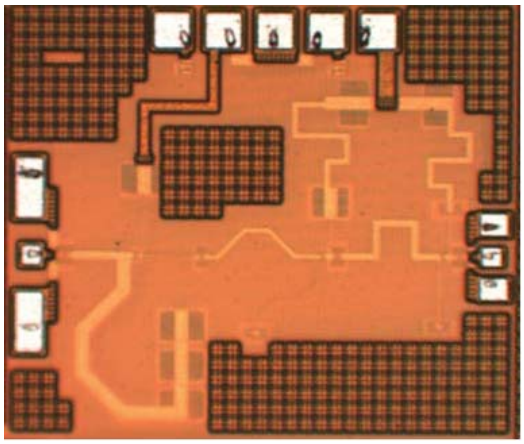


(c)

Figure 51: Performance Summary for 150 GHz Mixer (a), Simulated Output Power vs. Freq (b), and Swept Power (c)

4.2.1.3 Multiplier Breakout

The multiplier breakout includes a 60-to-120 GHz push-push doubler followed by an LO amplifier chain, with die photograph shown in Figure 52(a). Once again, all EM structures are custom designed. A performance summary table is shown in Figure 52(b). The simulated output power for the fundamental and second harmonic are shown in Figure 53(a) and 53(b) for final extracted simulations, indicating a conversion gain of 8 dB and a fundamental suppression of 25 dB.

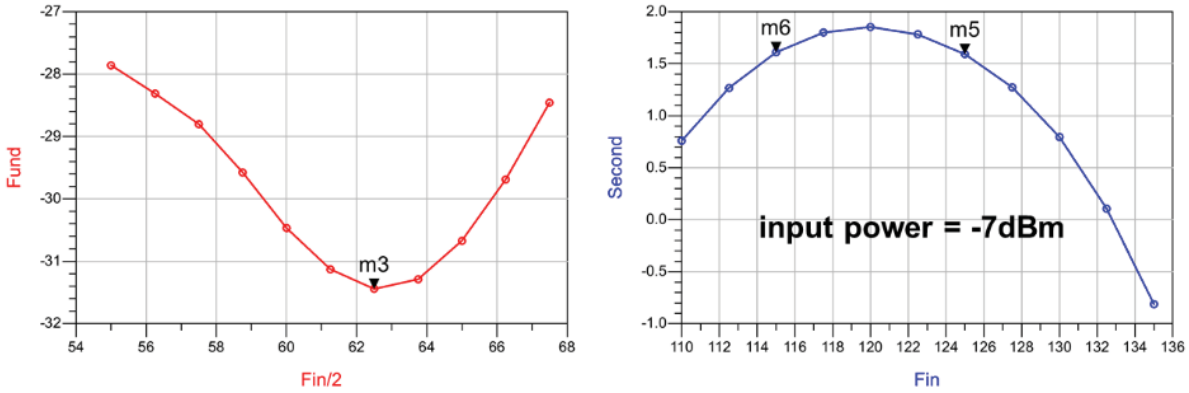


(a)

Performance Summary	
Conversion Gain	8dB
Tuning Range	110GHz – 135GHz
Output Power	1.5dBm
Fundamental Rejection	25dBc
LO Rejection	>30dBc
DC consumption	68mW
Area	850µmx750µm

(b)

Figure 52: Layout (a) and Performance Summary (b) of Multiplier



(a) (b)

Figure 53: Simulated Fundamental (a) and 2nd Harmonic (b) Output Power

4.2.2 Gen-1 150 GHz Measurements

Hardware for these designs were received in June 2017 and measurements were completed by August 2017. *These data show significant disagreement between models and hardware above 120 GHz for all circuits.*

4.2.2.1 150 GHz PA

NCSU does not own >110 GHz VNA extenders. As such, all of our >110 GHz measurements are scalar. The input signal is generated by a 12X Virginia Diodes, Inc. (VDI) frequency multiplier module which is driven by a signal generator. The module can output as high as 6 dBm over the 110-170 GHz frequency range. A manual variable attenuator is added after the VDI module to adjust the input signal to the chip. The total output power of the amplifier is measured with an Erickson calorimeter. Both input and output RF probes have WR5.1 waveguide interface and are specified to operate over the frequency range of 140-220 GHz. A WR5.1 to WR10 waveguide taper is used to match the output waveguide of the Erickson meter to the output RF probe. Prior to the measurement, the output power of the VDI module at different attenuator settings is measured with the power meter and stored as the input power to the chip. The effect of any impedance mismatch between the amplifier chip and VDI module is therefore neglected.

Insertion loss of the probes, pads and waveguide sections are calculated by measuring the loss of three 50 Ω transmission lines on the chip (L=200 μm, L=400 μm, L=800 μm) and extrapolating to L=0. The loss of two probes are estimated at 5 dB over 140-180 GHz and increases rapidly below 140 GHz to the cut-off frequency of the WR5.1 waveguides. The total loss of the taper and waveguide section before the power meter is estimated to be about 0.5 dB according to the VDI application note.

The measured power gain of the amplifier is shown in Figure 54 and compared to simulated results. Note that an update to transistor models were released at the time of layout submission and the original design was made with old models. Re-simulation with updated models show reduced gain of about 2 dB at 150 GHz. The measured gain is 8 dB which is lower than the 13.8 dB simulated gain by about 1.5 dB per stage. Other than the lower gain, the amplifier does not exhibit any major frequency shift, indicating good agreement for passives.

In an attempt to explain the lower measured gain an additional 1 Ω per unit length of the emitter fingers is added to the emitter of the transistor. This resistor value is chosen such that the simulated DC currents of the collectors match the simulated values. As can be seen in Figure 54 the amplifier gain with this added emitter resistance further drops to 11.7 dB.

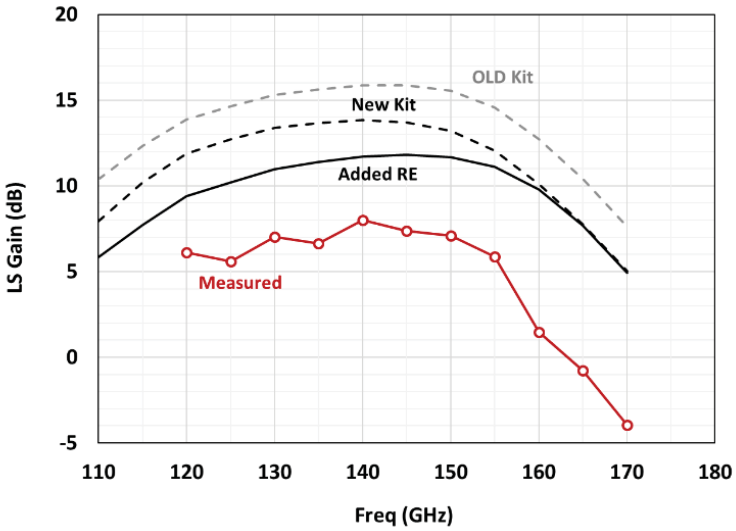


Figure 54: Measured (red) and Simulated (black) Power Gain of the Power Amplifier Chip

Figure 55 shows the comparison between measured and simulated output power of the amplifier at different frequencies. Lower gain is again visible in these plots. On the positive side, the amplifier does not seem to exhibit power compression up to the measured 7 dBm output power.

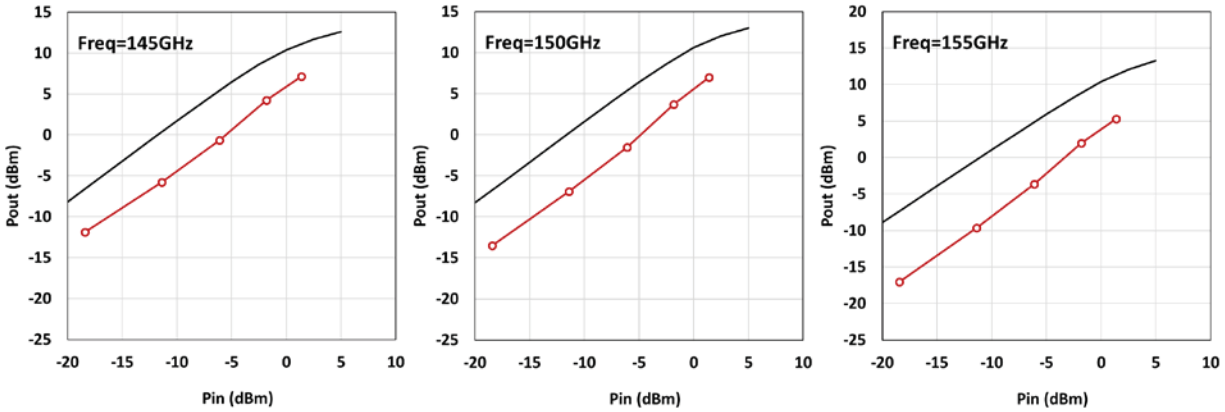


Figure 55: Measured (red) and Simulated (black) Output Power of the Amplifier vs. Input Power and Frequency

4.2.2.2 Broadband Cascode Amplifier

In an attempt to better understand the source of the lower gain, we measured another amplifier from an earlier tape-out in the same SiGe 9HP technology. The chip photograph of this three-stage cascode amplifier is shown in Figure 56. The amplifier is optimized for small-signal operation and uses smaller transistor sizes than the previous power amplifier. It also uses cascode transistors and therefore shows higher gain per stage compared to the previous design with common-emitter transistors.

As can be seen in Figure 56, the measured power gain (red) is closer to the simulated power gain (black solid line) up to 130 GHz but rapidly deviates at higher frequencies. This may be an indication that more accurate transistor models are indeed required to properly predict the performance of the circuits above 140 GHz. Simulated small-signal S_{21} of the amplifier is also shown in Figure 56 for reference.

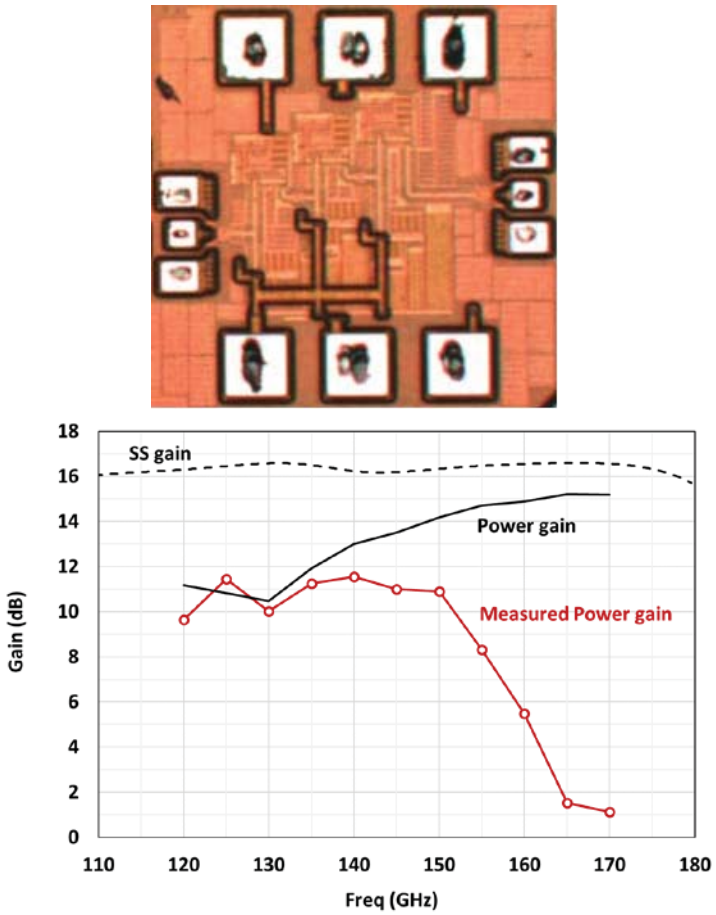


Figure 56: Chip Photograph of the Three-Stage Cascode Small-Signal Amplifier (top) and its Measured (red) and Simulated (black) Gain (bottom)

4.2.2.3 Up-Converting Balanced Mixer at 150GHz

In this mixer measurement setup, the LO signal is generated by the 12X VDI frequency multiplier chain and its level is controlled by the manual variable attenuator. The differential IF signals are generated with an off-chip balun. The output RF signal is measured with an X2-subharmonic mixer component. With this arrangement the spectrum analyzer is set up to operate with an external X12 mixer and its range is extended to 140-220 GHz.

Figure 57 shows the measured and simulated conversion gain and output power of the up-converting mixer chip with an IF frequency of 15 GHz and LO frequency of 150 to 165 GHz. With this frequency selection the lower sideband is 140-150 GHz. Note that the mixer is optimized to work with an LO frequency of 120 GHz and an IF frequency of 20-30 GHz. As can be seen in Figure 57, we again observe about 10 dB lower conversion gain for the mixer.

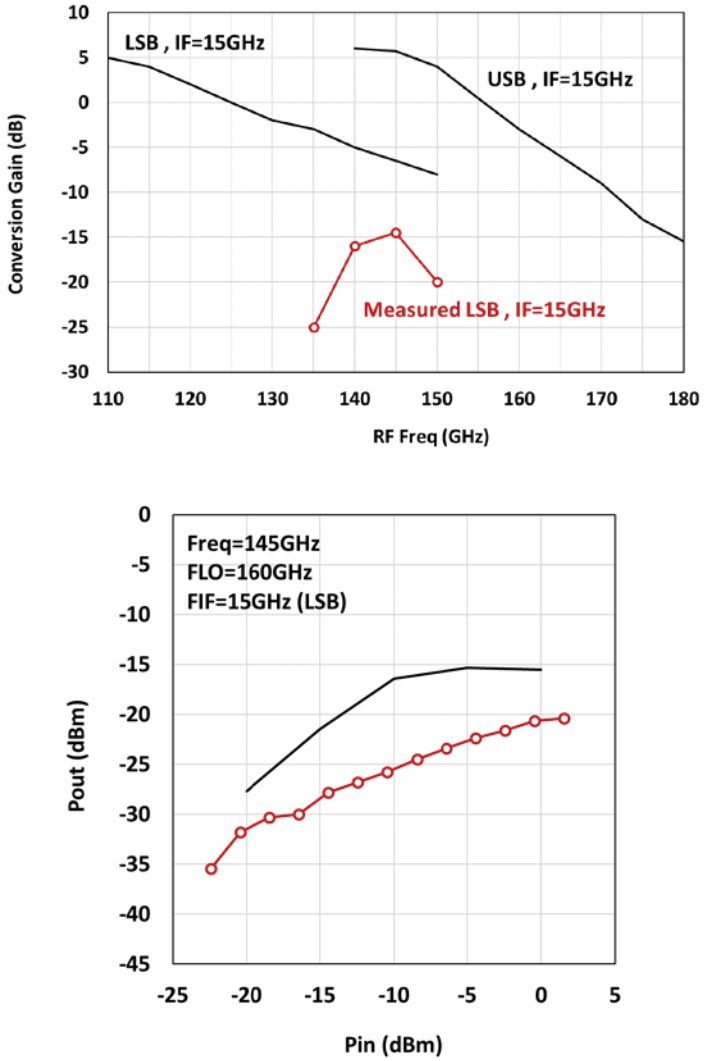


Figure 57: Measured (red) and Simulated (black) Conversion Gain and Output Power of the Mixer Chip

4.2.2.4 Frequency Doubler at 120GHz

In the doubler measurement setup, the input signal is generated with an X4 frequency multiplier and the total output power is measured with the Erickson meter. Due to the high-pass characteristics of the waveguides connected to the output, the measured total power is dominated by the second harmonic signal.

Figure 58 shows the measured vs. simulated output power and collector current of the frequency doubler versus frequency. During debugging the circuit, we also discovered a layout mistake, which was then taken into account. Although not accurate, this comparison gives us some indication that the frequency of the doubler has not shifted but similar to the previous circuits a power drop after 130 GHz is observed.

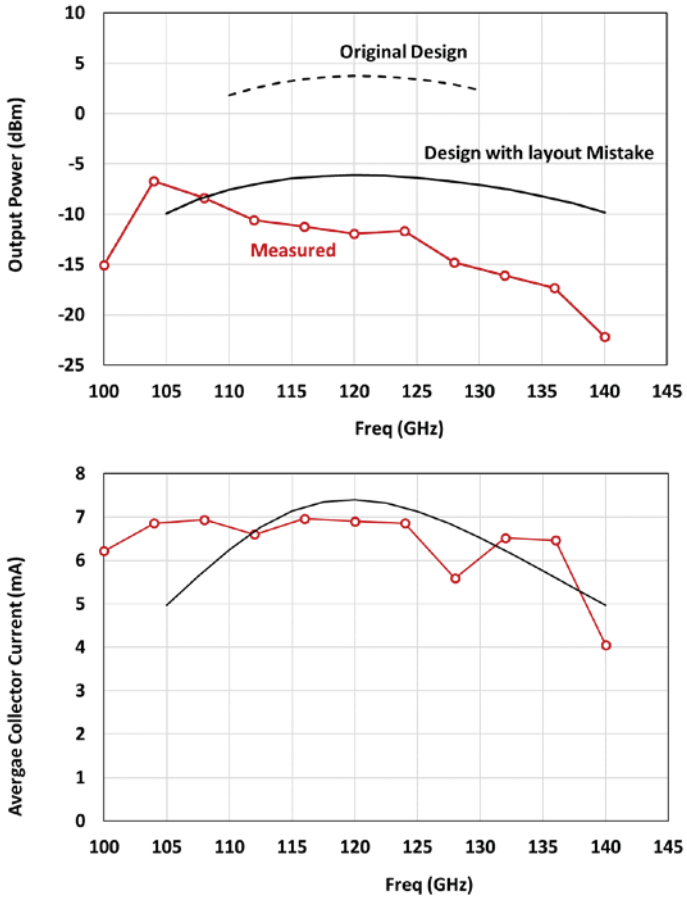


Figure 58: Measured (red) and Simulated (black) Output Power and Collector Current of the Frequency Multiplier

4.2.3 Gen-2 80 GHz Transmit EXTENDER Design

Due to the errors we observed with our 150 GHz transmitter components, we decided to shift our focus for Gen-2 to a lower frequency and a different technology. In particular, we estimated that obtaining good performance at 150 GHz would take two more tape-outs – one for revised components and another for full system. This would place this activity over budget and off schedule. As a result, we moved the Gen-2 transmit beamformer to 80 GHz in SiGe 8HP. We leveraged existing designs from Floyd's research group which had been fully characterized as part of a 76-81 GHz radar transceiver [Fuj17]. The Gen-2 EXTENDER was taped out in May 2018 in GF SiGe 8HP and is still being fabricated.

A block diagram of the transmitter is shown in Figure 59. It consists of an IF input of 25-27 GHz, which is within the range of our CORE transmitter. The LO is also 25-27 GHz which is in the range of the LO generated on the CORE. A frequency doubler generates LO for the up-conversion mixer. Finally, a multi-stage PA generates necessary output power for 76-81 GHz.

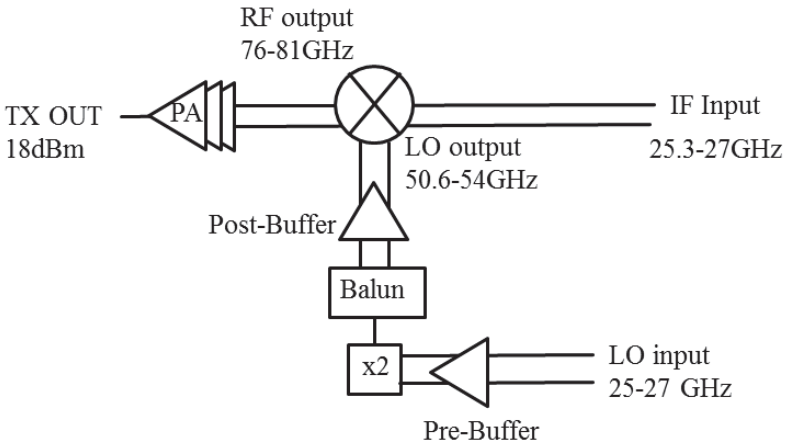


Figure 59: Block Diagram of the W-band Transmitter Element

Most of these blocks exist in a W-band radar transceiver realized in SiGe 8HP. These are re-used here to reduce risk and allow us to create a more sophisticated W-band extender. Note that this element does not include a phase shifter and instead focuses on TX chain performance (power, linearity, and bandwidth).

4.2.3.1 80 GHz Power Amplifier

The PA consists of three cascaded stages. Details on the PA can be found in [Fuj17] and a schematic of the final two stages is shown in Figure 60. The PA employs balanced cascodes biased in class-AB. The full PA chain generate a saturated output power of +16-18 dBm at 76 to 81 GHz.

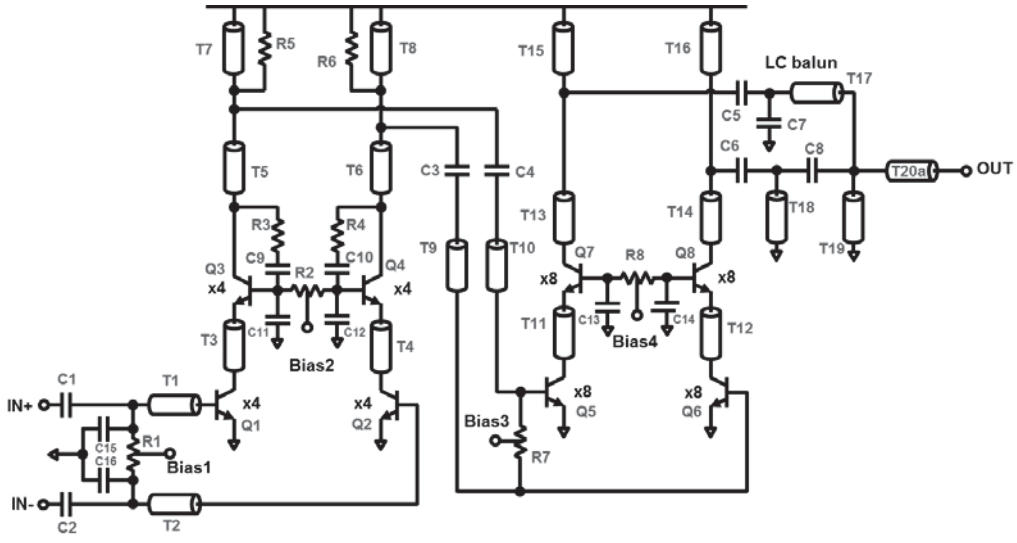


Figure 60: Schematic of 80 GHz PA

4.2.3.2 Upconversion Mixer

A double-balanced Gilbert mixer upconverts the 25-27 GHz IF input signal to an 80 GHz output signal. A schematic of the mixer is shown in Figure 61. The LO for this mixer is generated from a doubler chain described below. The mixer has a simulated voltage gain of 13 dB, for a 26 GHz input IF and 52 GHz LO frequency with -3 dBm LO power. It consumes 73 mW of power. The mixer RF and LO are matched using transmission line T-networks, where the shunt section is used to provide DC biasing. The IF is matched to 50 Ω using an inductive pi-network. Over the IF frequency range of 25-27 GHz, the mixer gain falls by less than 1 dB. The mixer provides a 1-dB output compression point of -1.4 dBm.

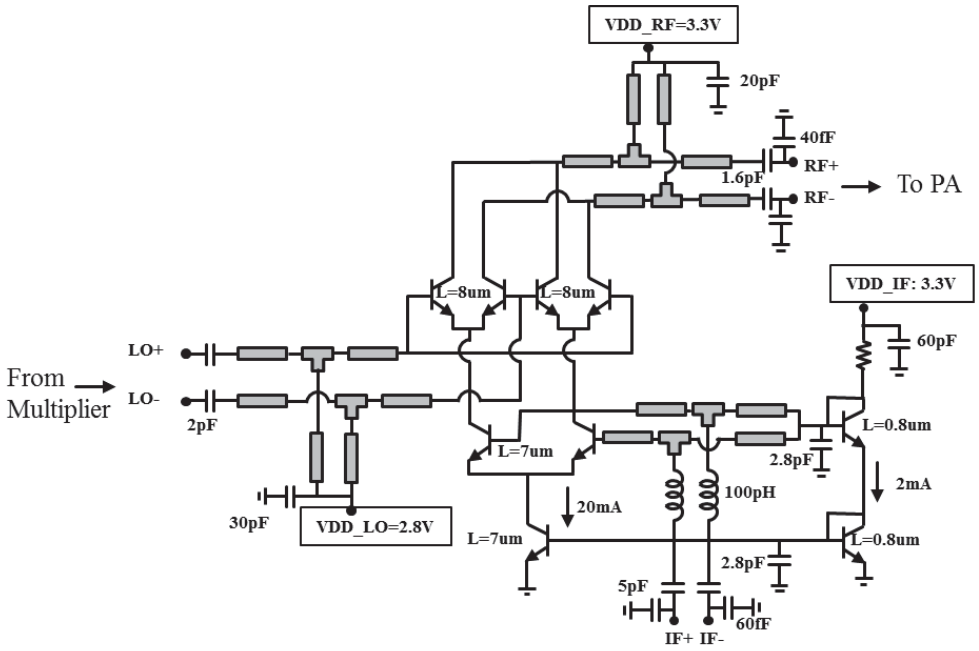


Figure 61: Schematic of 80 GHz Upconversion Mixer

4.2.3.3 Frequency Doubler with Buffers

A doubler is used to generate the LO signal for the mixer from the same clock signal used in the CORE transmitter. The 25-27 GHz input signal is first buffered. A schematic of the push-push doubler is shown in Figure 62. Following the doubler, a balun generates differential signal and then another buffer generates sufficient signal for the mixer. Both the pre-buffer and post-buffer use differential cascodes similar to the PA but tuned to the appropriate frequency. In simulation, the full cascaded buffer plus doubler chain can generate -3 dBm for an LO input power of +10 dBm.

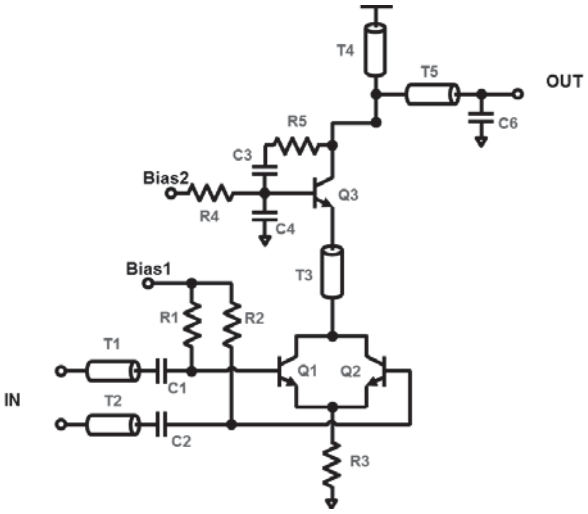


Figure 62: Schematic of 25 to 50 GHz Doubler

4.2.3.4 Simulated Results of 80 GHz EXTENDER

The complete transmitter EXTENDER chain layout is shown in Figure 63. The simulated results are summarized here. Complete gain through the RF path is 22 dB. The output saturated power is +16 dBm. A representative matching and swept power simulation (screenshots) are shown in Figures 64 and 65, indicating that the device is well matched at the ports and provides the before mentioned power gain and output power.

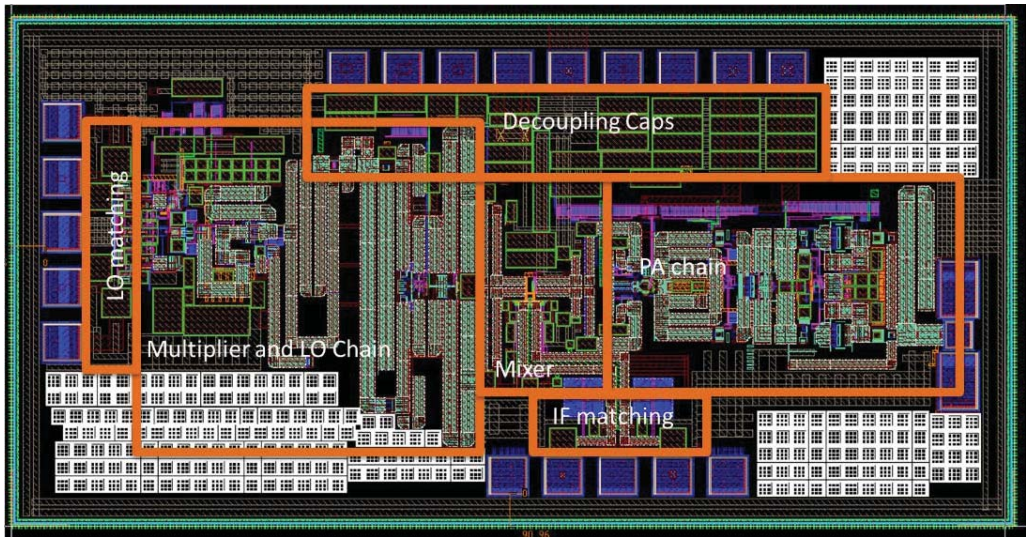


Figure 63: Layout of the complete Gen-2 80-GHz EXTENDER in SiGe 8HP

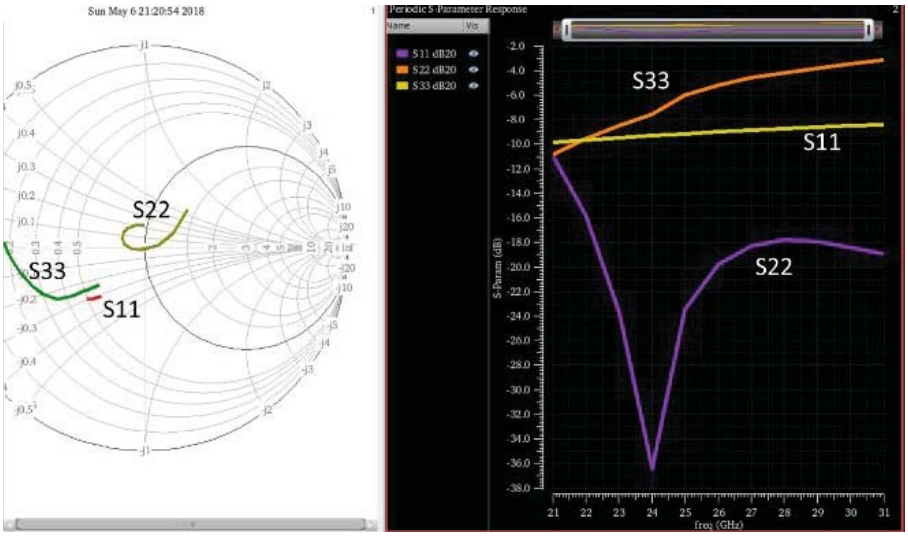


Figure 64: Simulated Reflection Coefficients of the Full Transmitter Chain
Port 1 is LO at 42-62 GHz, Port 2 is IF at 21-31 GHz, Port 3 is RF at 63-93 GHz.

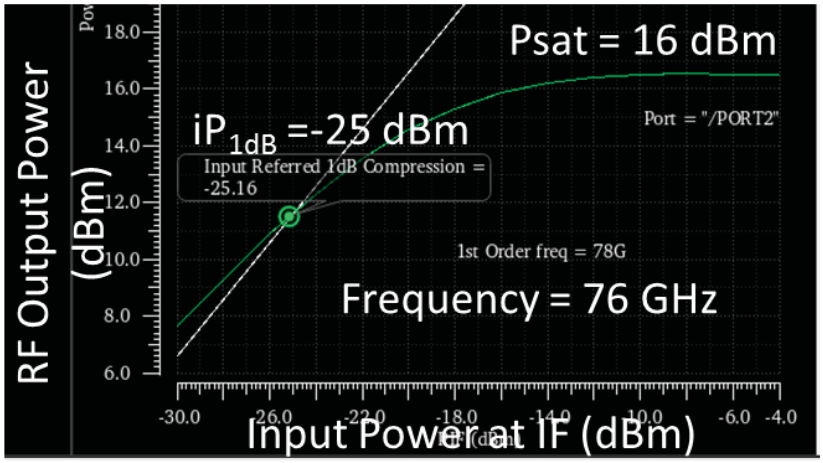


Figure 65: Simulated Swept Power Response of Full Transmitter Chain

4.2.4 Gen-2 80 GHz EXTENDER Measurements

The Gen-2 EXTENDER was taped out in May 2018. It is still being manufactured with expected delivery to NCSU in September 2018. It will be characterized at chip level in September/October 2018 timeframe.

4.3 Thrust 2C (60 GHz EXTENDER)

We completed wafer-level characterization of our 60 GHz four-element receive beamformer which was implemented in TowerJazz SBC18H3 SiGe BiCMOS technology. Figure 66(a) and 66(b) show a block diagram and photo of the beamformer. A four-element receiver is integrated together with a parallel combining network. Built-in test capabilities are included to allow measurement of each receive chain's amplitude and phase response in parallel using code-modulation techniques. Each front end includes an LNA and a phase shifter. The measured amplitude and phase responses are shown in Figure 66(c) and 66(d) for six-bit control.

Extremely uniform performance is seen across frequency with low root-mean-squared (RMS) gain and phase errors across the full 57-67 GHz band. Additionally, all code-modulated built-in self-test capabilities work as expected. Gain, NF, and power consumption results are summarized inset to Figure 66. Further details on this circuit and built-in self-test (BIST) can be found in [Gre18].

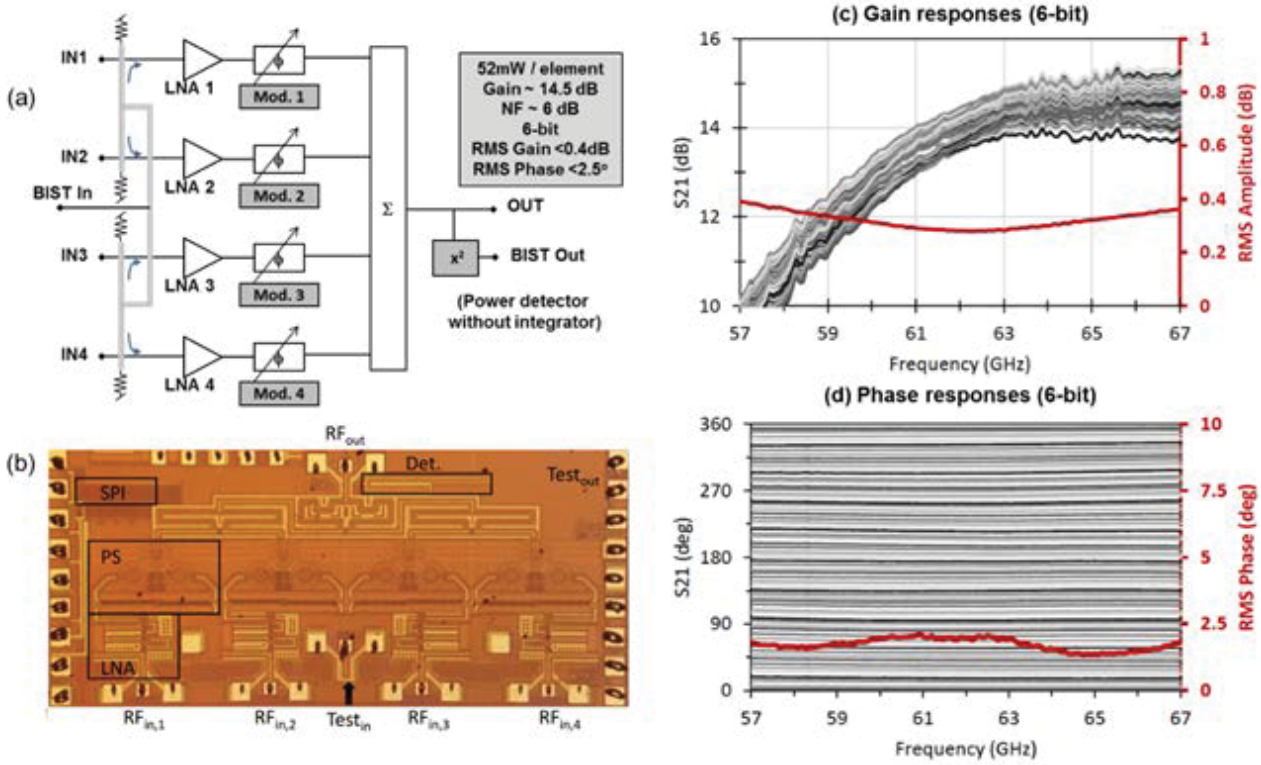


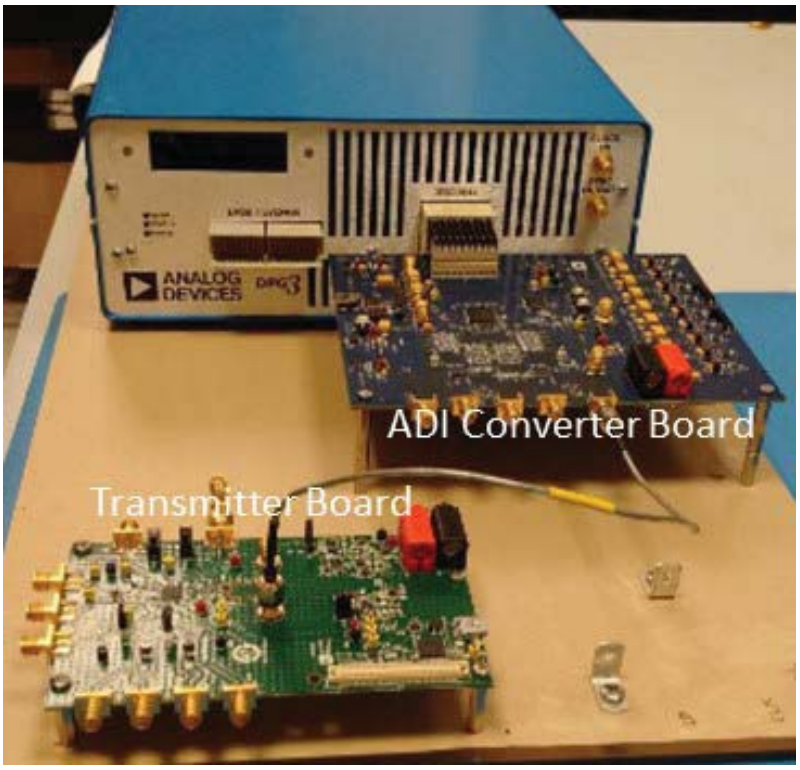
Figure 66: Block Diagram of 60 GHz receive beamformer implemented in TowerJazz SBC18H3 (a), Die Photograph (b), Measured 6-bit Gain Response (c), Measured 6-bit Phase Response (d)

5. THRUST 3: PHASED-ARRAY PLATFORMS

The goal of this thrust is to evaluate phased-array PLATFORMS comprising the multi-purpose IP CORE and mm-wave EXTENDERS. Performance will be evaluated according to program metrics.

5.1 Testbed Development

We created test benches for measurement of transmitters and receivers. For the transmitter, the baseband is based on a custom data converter chipset from Analog Devices, Inc. (ADI), mounted on a board and connectorized to allow us to generate arbitrary baseband in-phase and quadrature-phase waveforms. We have developed custom digital signal processing (DSP) software to be able to program the modulation format, pulse shapes, etc. These waveforms can be used to directly control the transmitter or they can be externally up-converted to 28 GHz to provide signals for the receiver. An example screenshot of the resulting 16-QAM waveforms are shown in Figure 67. To characterize the output of the transmitter or the baseband outputs of the receiver, we will use our real-time oscilloscope and then digitally demodulate the signals.



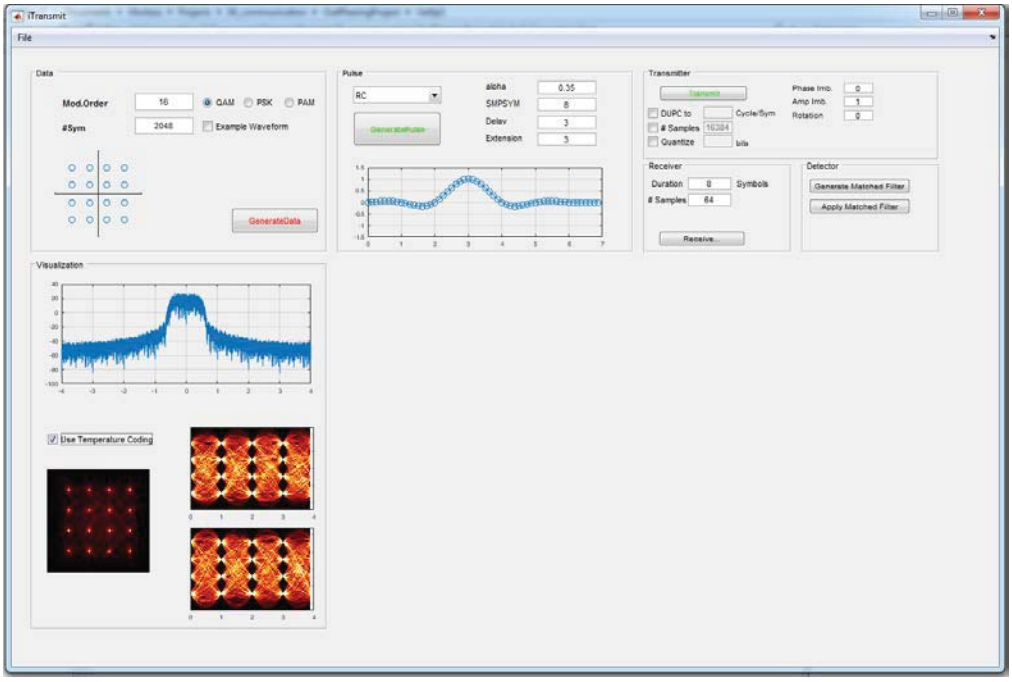


Figure 67: Custom Baseband Generator from ADI (top) and the DSP Software developed at NCSU for a 16-QAM Signal (bottom)

5.2 Full Platforms

Progress on this thrust has been hampered by the following. First, the PLATFORM requires both functional COREs and functional EXTENDERS. As discussed previously, it is only our final generation (Gen-2) receiver and transmitter COREs which provide the required and envisioned capabilities. Our Gen-2 receiver CORE was received in summer 2018 with most measurements completed in August 2018. As a result, we have not yet been able to package this receiver and incorporate it with an EXTENDER. These activities are in progress, where we have designed the boards and will now proceed to assembly and test.

For the CORE transmitter, our Gen-2 circuit was taped out in May 2018 ad is still in fabrication. It should be available to us in the September/October 2018 time frame, at which time we will conduct transmitter measurements. Therefore, we will proceed to PLATFORM assembly of the transmitter in November 2018.

For our EXTENDERS, the 28 GHz beamformer (receiver and transmitter) is available and fully characterized. Likewise, the 60 GHz receive beamformer is available and fully characterized. Our 80 GHz transmit beamformer is still in fabrication (May 2018) tape-out. Its time frame for test and assembly mirrors that described for the Gen-2 transmitter CORE above.

Additionally, our progress related to packaging and assembly has been slowed down by the departure of the Thrust 3 leader, Morteza Abbasi, in December 2017. As a result, these work tasks have been reassigned among our research team, including the students who designed the COREs, as well as visiting scholars who have joined Floyd's research group having background in mm-wave packaging and board design.

5.3 Plans for Completing Final Platform Measurements

It is possible to predict the performance of the overall PLATFORMs using the individual measured or simulated performance of COREs and EXTENDERs. However, we refrain from doing so here, as these predictions should mirror those given in our original proposal. This is because our CORE is achieving the desired original program targets. As a result, we will wait to show any PLATFORM data once the full systems are assembled and tested.

Our experimental plans for the PLATFORM include three test cases, as follows:

(1) Evaluation of 28-GHz EXTENDER RX or TX (from our ADI project, under Thrust 2A) with our CORE in mode 1. Here, we will package our 28-GHz four-element phased-array developed in parallel in our ADI project with the EPIC CORE. A complete PCB for the 28 GHz phased array is ready and designed. The 28GHz interface will be a board-level interconnect. The 28 GHz outputs of the array will be probed.

(2) Evaluation of 60-GHz EXTENDER RX (from our Samsung project, under Thrust 2C) with our CORE in mode 3. Based on the subharmonic performance of our Gen-1 CORE, we do not expect this to produce useful results; however, we will still evaluate the subharmonic performance of the Gen-2 CORE to see if the conclusion is any different. If so, then we will proceed to create this 60 GHz platform.

(3) Evaluation of 80-GHz EXTENDER TX (under Thrust 2B) with our CORE in mode 2. For this activity, we will create a PCB for the core TX and extender. The interface between the two will be a transmission line on the PCB. The 80 GHz transmitter output will be wafer probed.

For packaging, we plan to use chip-on-board with wirebonding. Simulations indicate that we can use wirebonding between the silicon die and the Duroid substrate without major signal degradation.

5.4 Final Reporting and Deliverable

Since our PLATFORM work will continue beyond the period of this contract, we plan to release a supplement to this final report once that work is completed along with the hardware deliverables. Furthermore, since this seedling has led to the demonstration of useful receiver COREs which form the foundation of an upcoming DARPA MIDAS effort, we realized that we will have continuity with DARPA, providing a natural way to continue providing updates on the EPIC results.

6. MANAGEMENT SUMMARY

6.1 Program Challenges

As discussed previously, there were numerous challenges encountered while managing the program. First, we encountered technical challenges in (a) the design of our CORE transceiver which resulted in additional hardware iterations and (b) the design of our highest frequency EXTENDER which resulted in shifting from 150 GHz to 80 GHz to allow re-use of existing hardware blocks. The schedule still delayed as a result.

Second, we encountered significant PDK challenges for 45nm RFSOI from GF. This included a shift from IBM's CMOS-12S PDK to GFs first 45RFSOI PDK, a shift to a revised GF 45RFSOI PDK in which mm-wave enablement was introduced which replaced some of our custom components, and a shift to a new required metal stack in GF 45RFSOI. Altogether, this led to postponed tape-outs and significant repeated work, costing about six months of development time. Consequentially, the final version of our transmitter CORE is still in fabrication.

Finally, we encountered staffing challenges, where the Thrust 3 platform leader, research professor Morteza Abbasi left NCSU in December 2017. His expertise included mm-wave packaging and assembly and full system evaluation. As a result of this, as well as the status of our transceiver CORE, we have not yet demonstrated assembled phased-array platforms.

6.2 Staffing

Prof. Brian Floyd served as the principal investigator and supervised Thrust 1, 2A, and 2C. Thrust 2B was supervised by Prof. David Ricketts. Thrust 3 was supervised by Dr. Morteza Abbasi until his departure in December 2017. It was then supervised by Prof. Brian Floyd. Multiple researchers and Ph.D. students worked on this project, with roles as follows.

- Under Thrust 1, we had four students. Sandeep Hari was responsible for receiver core design and all LO networks. Tiantong Ren was responsible for the transmitter core and PA design. Vikas Chauhan was responsible for the LNA design. Avinash Bhat was responsible for the analog baseband design.
- Under Thrust 2, we had five students and researchers. Yi-Shin Yeh was responsible for the 28 GHz transceiver array. Kevin Greene and Vikas Chauhan were responsible for the 60 GHz receiver array. Morteza Abbasi and Deeksha Lal were responsible for 150 GHz component design. Deeksha Lal was responsible for 80 GHz extender design.
- Under Thrust 3, we had three researchers. Morteza Abassi was responsible for testbed development and all original packaging and assembly plans. Sandeep Hari took over responsibility for 28 GHz and 60 GHz receiver platform demonstrations. Tiantong Ren took over responsibility for 28 GHz and 80 GHz transmitter platform demonstrations.

7. REFERENCES

Note that the publications marked with ** are related to the EPIC program. These are attached as an Appendix to this report within the PDF version.

[And10] C. Andrews and A. C. Molnar, "Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers," *IEEE Trans. Circuits Systems I: Regular Papers*, vol. 57, no. 12, pp. 3092-3103, Dec. 2010.

[Cha18] **V. Chauhan and B. Floyd, "A 24-44GHz UWB LNA for 5G cellular frequency bands," *IEEE Global Symp. Millimeter-Waves*, May 2018.

[Fuj17] T. Fujibayashi, Y. Takeda, Y.-S. Yeh, W. Wang, W. Stapelbroek, S. Takeuchi, and B. Floyd, "A 76 to 81 GHz multi-channel radar transceiver," *IEEE J. Solid-State Circuits*, vol.52, no.9, pp.2226-2241, Sep. 2017.

[Gree18] **K. Greene, V. Chauhan, and B. Floyd, "Built-in-test of phased arrays using code-modulated interferometry," *IEEE Trans. Microw. Theory Tech.*, vol. 66, no. 5, pp. 2463-2479, May 2018.

[Wil16] C. Wilson and B. A. Floyd, "A 20-30 GHz mixer-first receiver in 45-nm SOI CMOS," *IEEE RFIC Symp*. May 2016, pp. 344-347.

[Wil18] C. Wilson and B. Floyd, "Harmonic performance of mixer-first receiver with circulant-symmetric baseband," *IEEE Trans. Circuits Systems-I: Reg. Papers*, doi: 10.1109/TCSI.2018.2856257.

[Yan15] D. Yang, C. Andrews, and A. Molnar, "Optimized design of N-phase passive mixer-first receivers in wideband operation," *IEEE Trans. Circuits Systems-I: Reg. Papers*, vol. 62, no. 11, Nov. 2015.

[Yeh17] **Y.-S. Yeh, E. Balboni, and B. Floyd, "A 28-GHz phased-array transceiver with series-fed dual-vector distributed beamforming," IEEE RF Integrated Circuits Symp., June 2017.

LIST OF SYMBOLS, ABBREVIATIONS, AND ACROYNMS

ACRONYM	DESCRIPTION
ADI	Analog Devices, Inc.
BB	baseband
BIST	built-in self-test
CML	current-mode logic
CMOS	complementary metal-oxide-semiconductor
DAC	digital-to-analog converter
DARPA	Defense Advanced Research Projects Agency
DC	direct current
DSP	digital signal processing
EM	electromagnetic
EPIC	Extendable phased-array Platform ICs
EVM	error vector magnitude
FET	field-effect transistor
GF	GlobalFoundries
GSMM	Global Symposium on Millimeter Waves
I and Q	in-phase and quadrature
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
IP	intellectual property
iP_{1dB}	input one-dB compression point
IRR	image rejection ratio
LNA	low-noise amplifier
LNTA	low-noise transconductor amplifier
LO	local oscillator
MIDAS	Millimeter-Wave Digital Arrays
MIM	metal-insulator-metal
MOSFET	metal-oxide semiconductor field-effect transistor
NCSU	North Carolina State University
NF	noise figure
NF_{dsb}	double-sideband noise figure
PA	power amplifier
PAE	power added efficiency
PCB	printed circuit board
PDK	process design kit
RF	radio frequency
RMS	root-mean-squared
SOI	silicon-on-insulator
SPI	serial peripheral interface
SRC	Semiconductor Research Corporation
TIA	transimpedance amplifier
t-line	transmission line
VDI	Virginia Diodes, Inc.
VGA	variable-gain amplifier

ACRONYM	DESCRIPTION
VNA	vector network analyzer
VNCAP	vertically natural capacitor